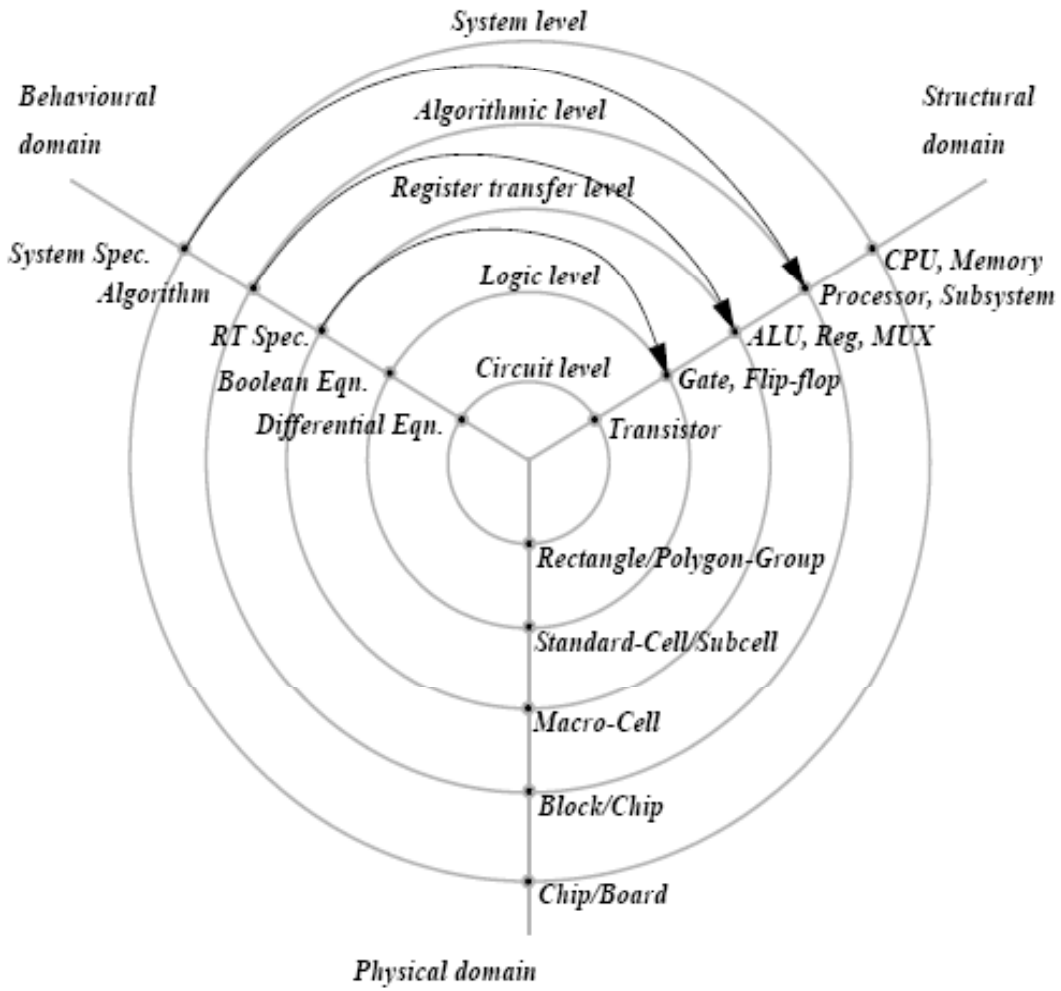
Review of MOS Technology

Review of MOS technology

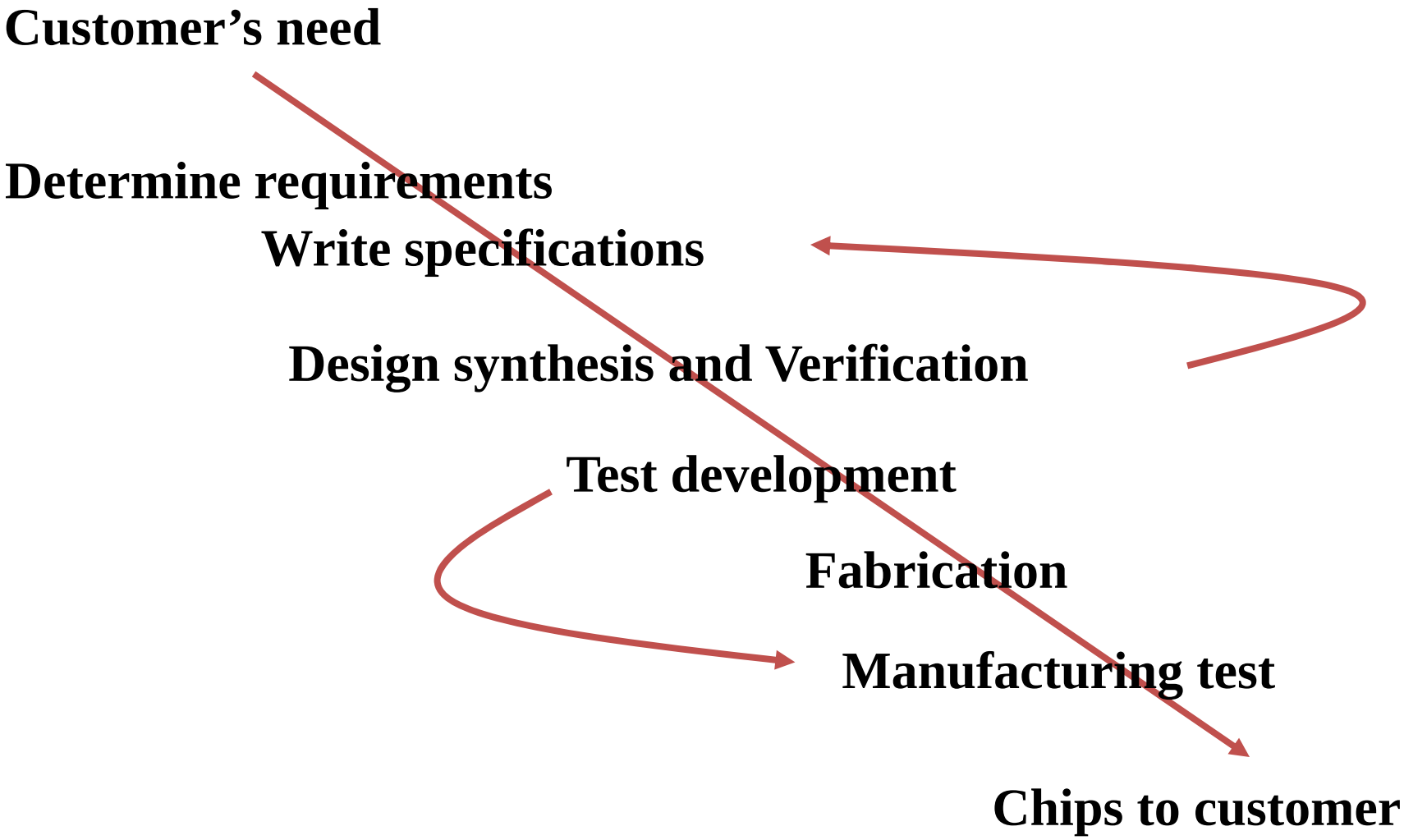
- Basic MOS Transistors,
- Enhancement and Depletion mode transistors,
- N MOS and CMOS process,
- Thermal aspects of processing,
- Production of masks.

Types of Synthesis

- *Behaviour to Structure*
  - *System*
  - *Algorithmic*
  - *FSM/Logic*
  - *Circuit*
- *Structure to Layout*
  - *System Partitioning*
  - *Chip Floorplanning*
  - *Module generation*
  - *Cell generation*



VLSI Realization Process



Reliability of Integrated Circuits

- Design and verification
  - Important part before the product is taped out
- Manufacturing test
  - Generally determines the quality and reliability
  - Various tests are performed using numerous methods
    - Structural test
    - Functional test
    - Power consumption test

Verification vs. Test

Verification

- Verifies correctness of design.
- Performed by simulation, formal methods.
- Performed once prior to manufacturing.
- Responsible for quality of design.

Test

- Verifies correctness of manufactured hardware.
- Two-part process:
  1. Test generation: software process executed once during design
  2. Test application: electrical tests applied to hardware
- Test application performed on every manufactured device.
- Responsible for quality of devices.

M O S F E T

Metal Oxide Semiconductor Field Effect Transistor

FET

FET's (Field – Effect Transistors) are much like BJT's (Bipolar Junction Transistors).

Similarities:

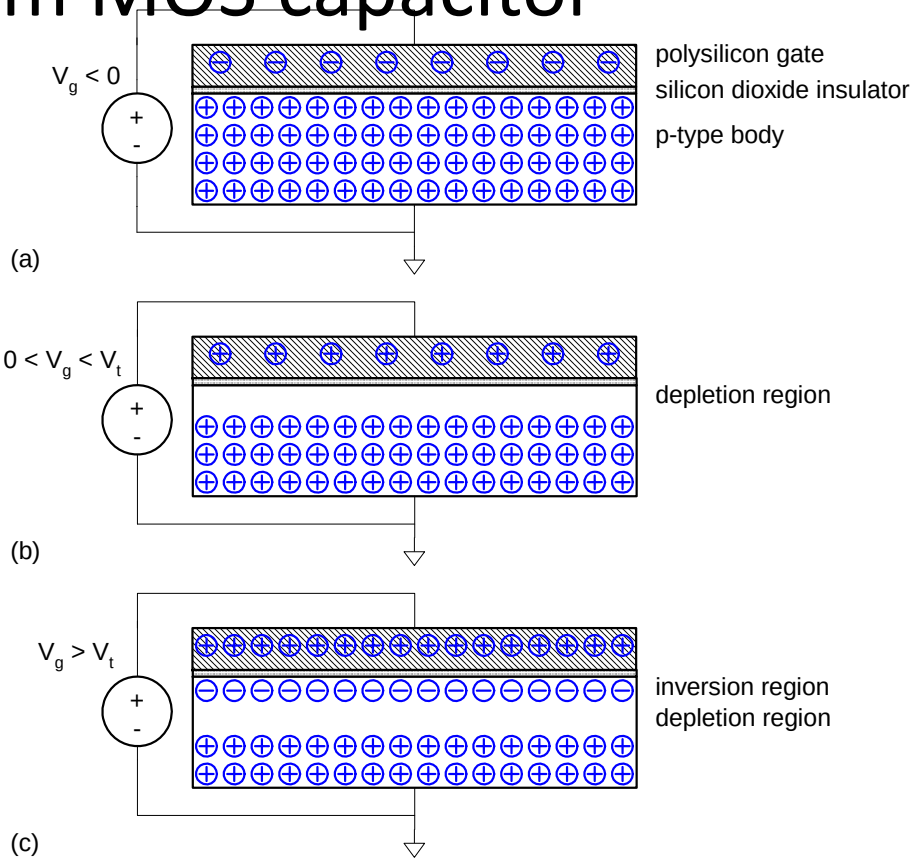
- **Amplifiers**
- **Switching devices**
- **Impedance matching circuits**

Differences:

- **FET's are voltage controlled devices whereas BJT's are current controlled devices.**
- **FET's also have a higher input impedance, but BJT's have higher gains.**
- **FET's are less sensitive to temperature variations and because of there construction they are more easily integrated on IC's.**
- **FET's are also generally more static sensitive than BJT's.**

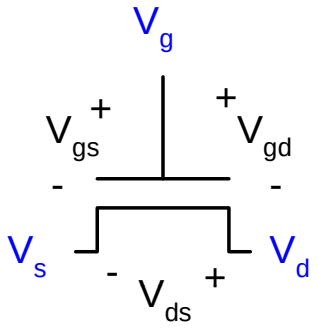
MOS Capacitor

- Gate and body form MOS capacitor
- Operating modes
  - Accumulation
  - Depletion
  - Inversion



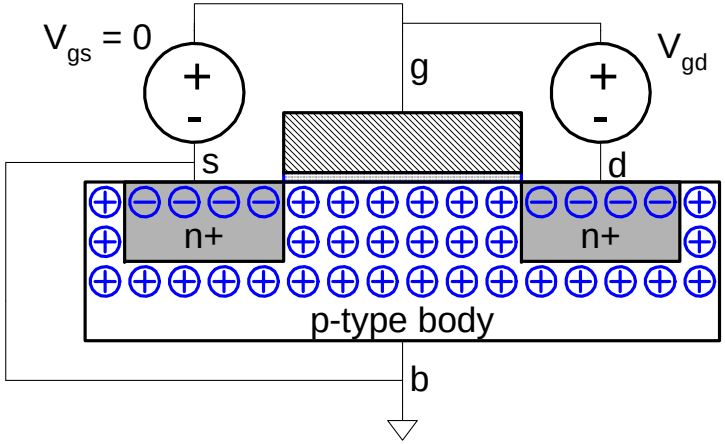
Terminal Voltages

- Mode of operation depends on V_g, V_d, V_s
  - $V_{gs} = V_g - V_s$
  - $V_{gd} = V_g - V_d$
  - $V_{ds} = V_d - V_s = V_{gs} - V_{gd}$
- Source and drain are symmetric diffusion terminals
  - By convention, source is terminal at lower voltage
  - Hence $V_{ds} \geq 0$
- nMOS body is grounded. First assume source is 0 too.
- Three regions of operation
  - *Cutoff*
  - *Linear*
  - *Saturation*



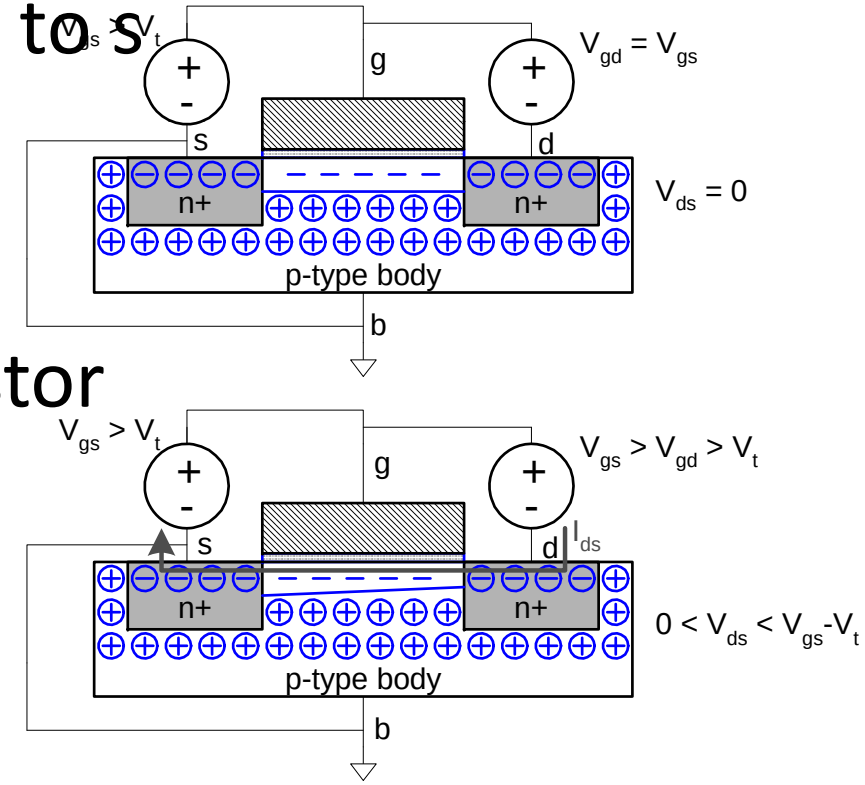
nMOS Cutoff

- No channel
- $I_{ds} = 0$



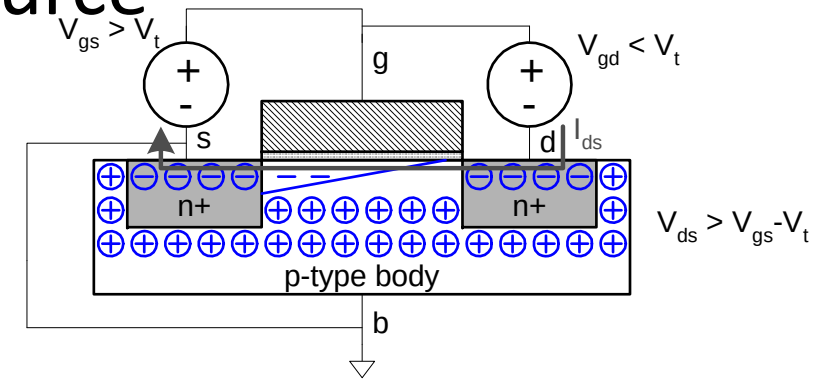
nMOS Linear

- Channel forms
- Current flows from d to s
  - e^- from s to d
- I_{ds} increases with V_{ds}
- Similar to linear resistor



nMOS Saturation

- Channel pinches off
- I_{ds} independent of V_{ds}
- We say current saturates
- Similar to current source



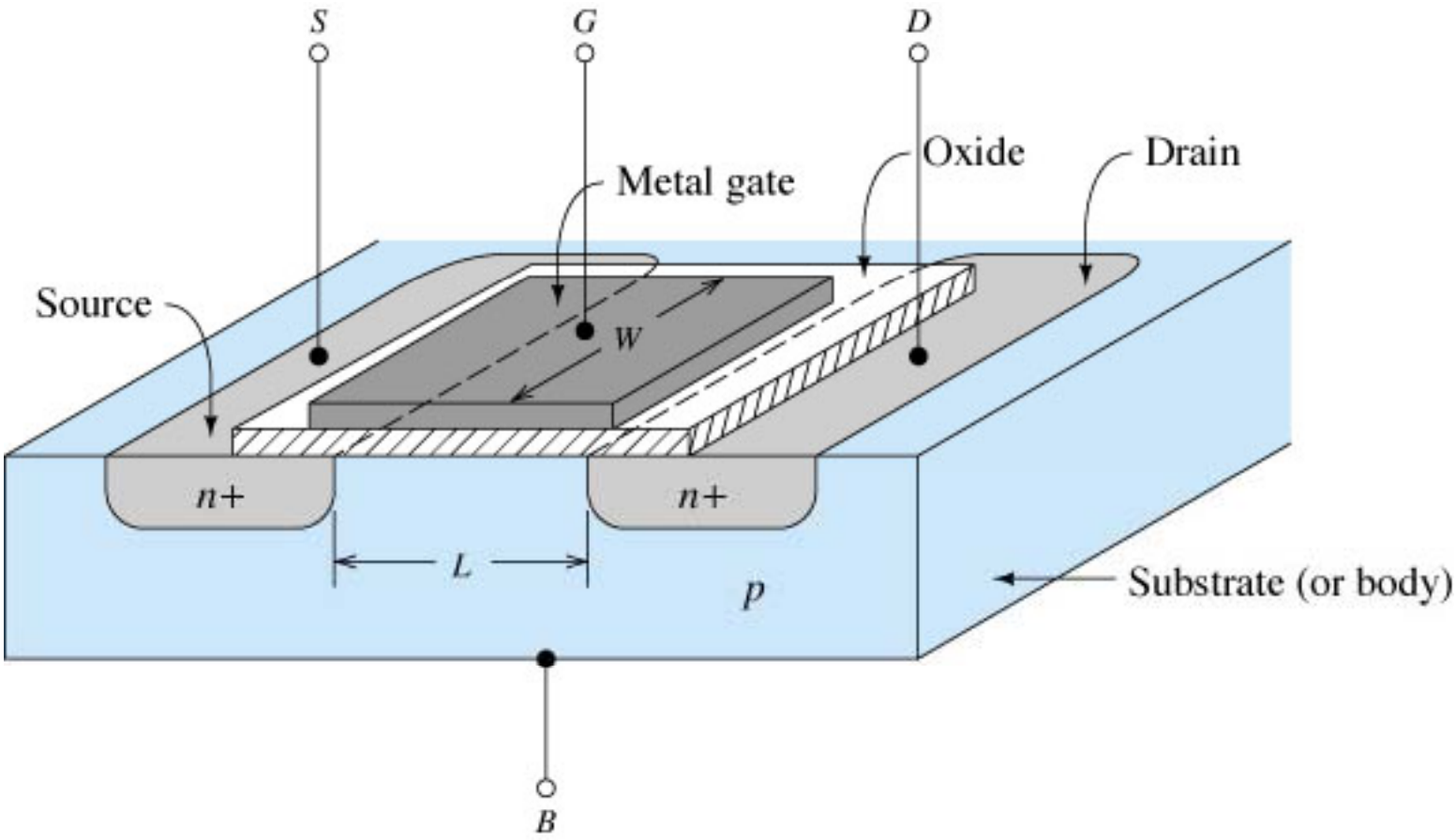
MOSFET's

MOSFETs have characteristics similar to JFETs and additional characteristics that make then very useful

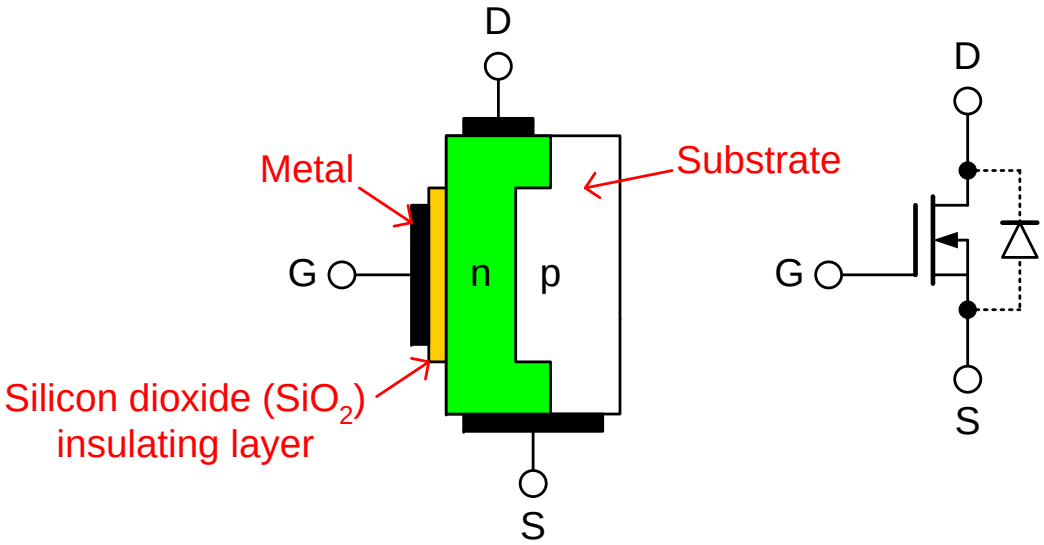
There are 2 types of MOSFET's:

- **Depletion mode MOSFET (D-MOSFET)**
  - **Operates in Depletion mode the same way as a JFET when VGS ≤ 0**
  - **Operates in Enhancement mode like E-MOSFET when VGS > 0**
- **Enhancement Mode MOSFET (E-MOSFET)**
  - **Operates in Enhancement mode**
  - **IDSS = 0 until VGS > VT (threshold voltage)**

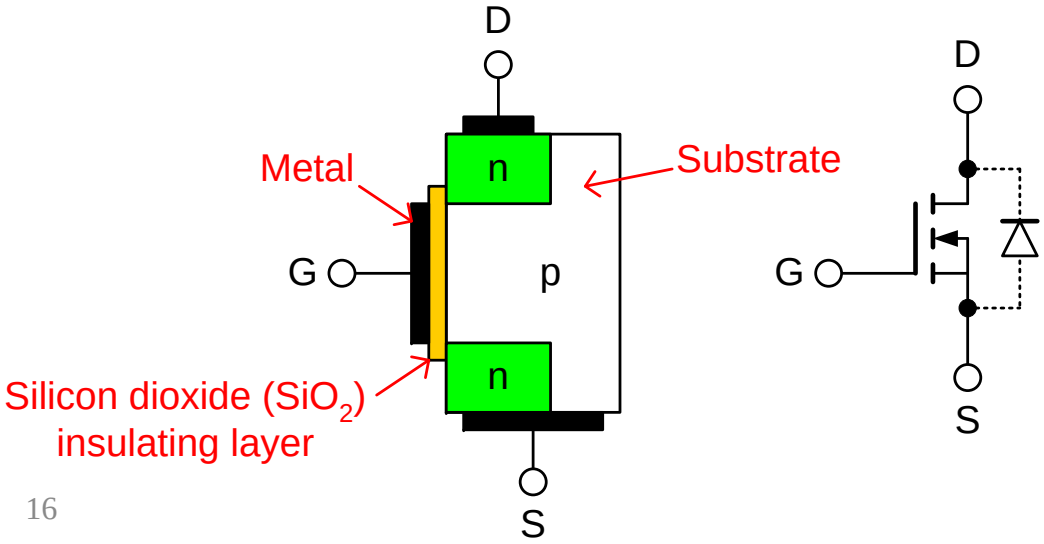
n-Channel E-MOSFET showing channel length L and channel width W



n-channel MOSFET.

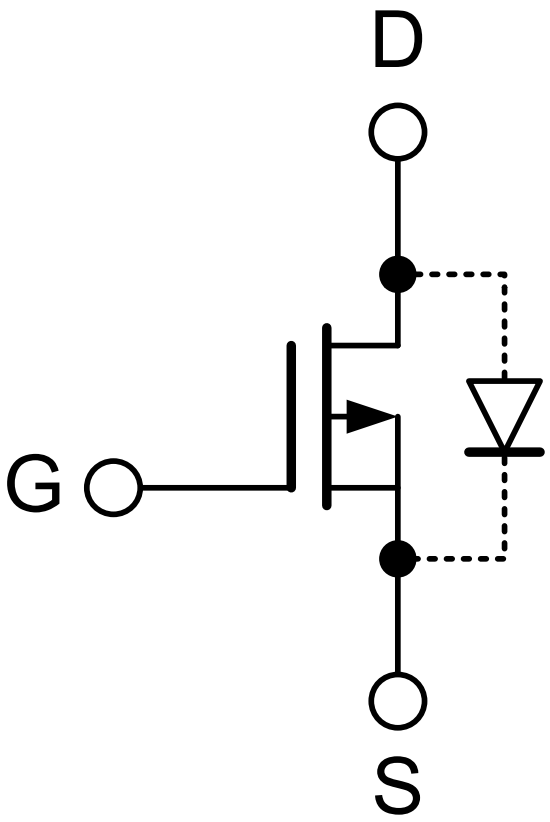


Depletion-type MOSFET (D-MOSFET)

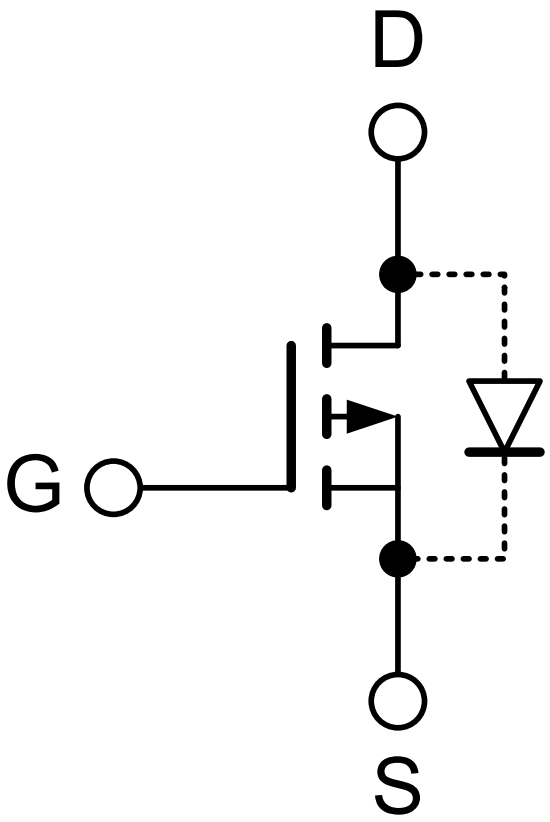


Enhancement-type MOSFET (E-MOSFET)

p-channel MOSFET

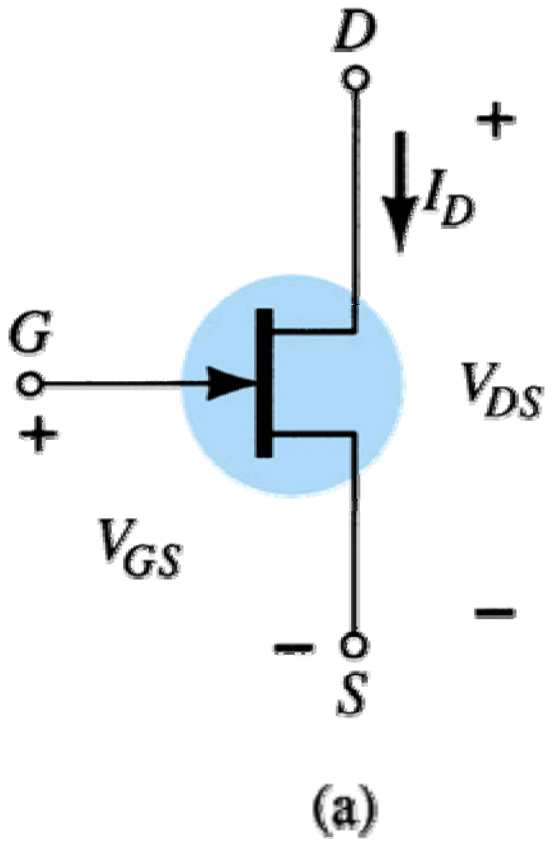


Depletion-type MOSFET (D-MOSFET)

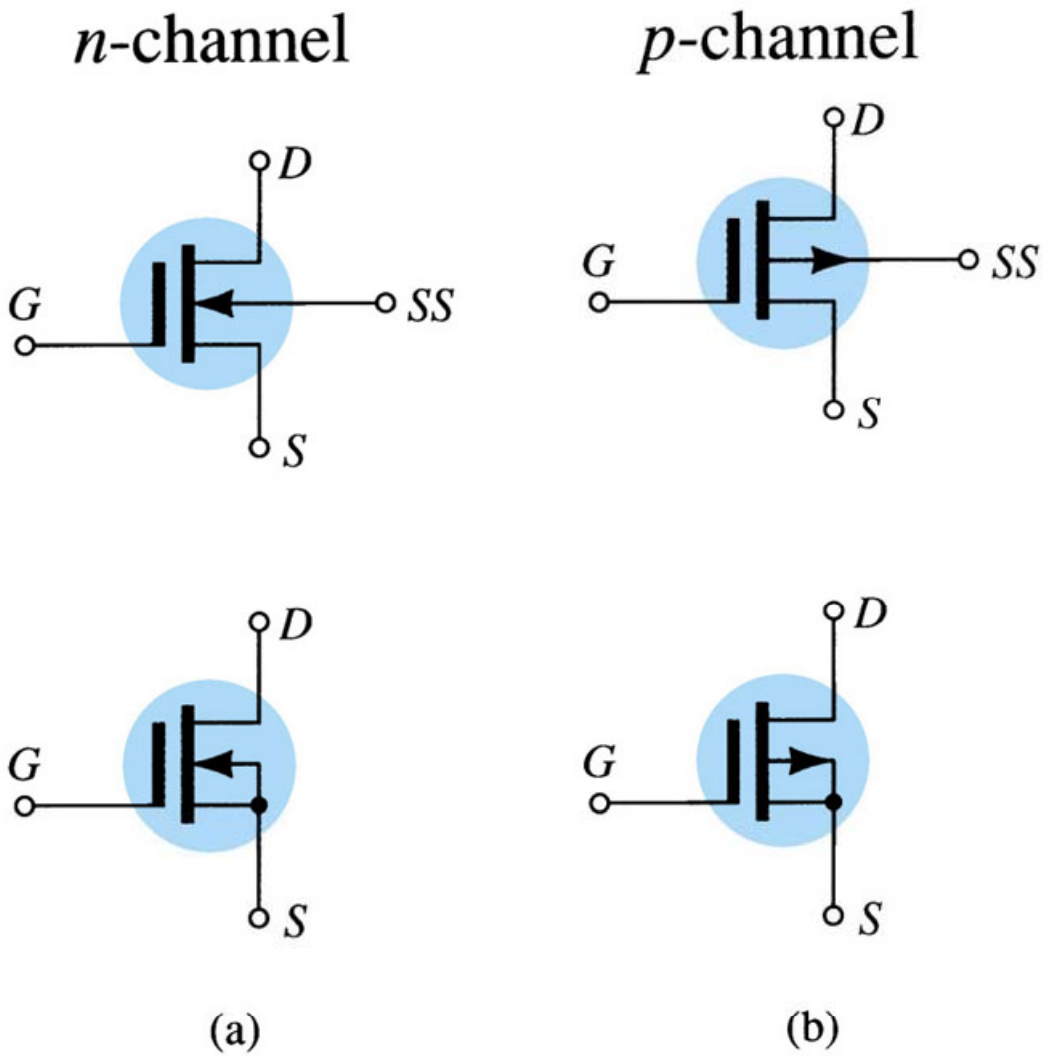


Enhancement-type MOSFET (E-MOSFET)

MOSFET Symbols



Symbols



MOSFET Operating Characteristics

- **Cutoff Region: Where the current flow is essentially (Accumulator Region)**

$$V_{DS} = 0 \; ; \; V_{GS} < V_t$$

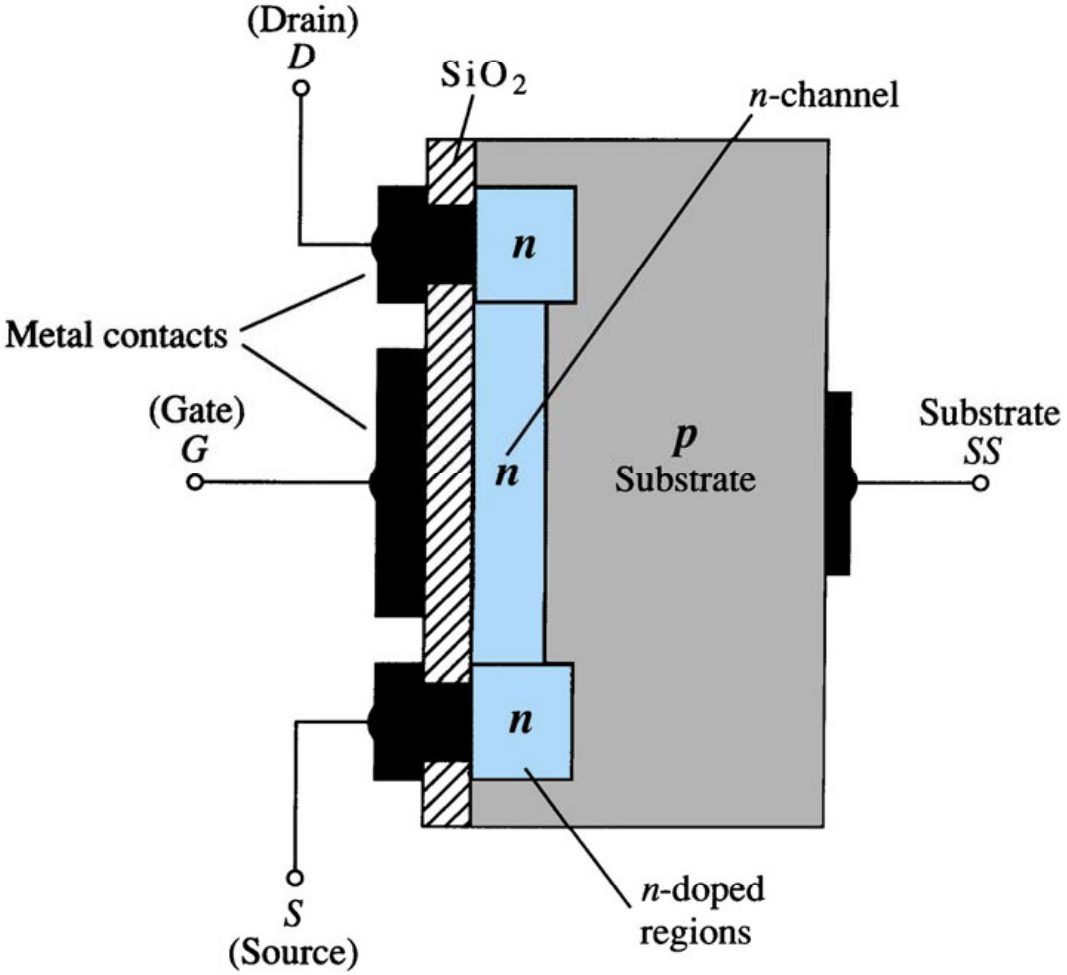
- **Non-saturated Region: Weak inversion region where the drain current is dependent on the gate and drain voltage (w.r.t. substrate).**

$$V_{DS} < V_{GS} - V_t$$

- **Saturated Region : Channel is strongly involved and drain current flow is ideally independent of the drain-source voltage (Inversion)**

$$V_{DS} > V_{GS} - V_t$$

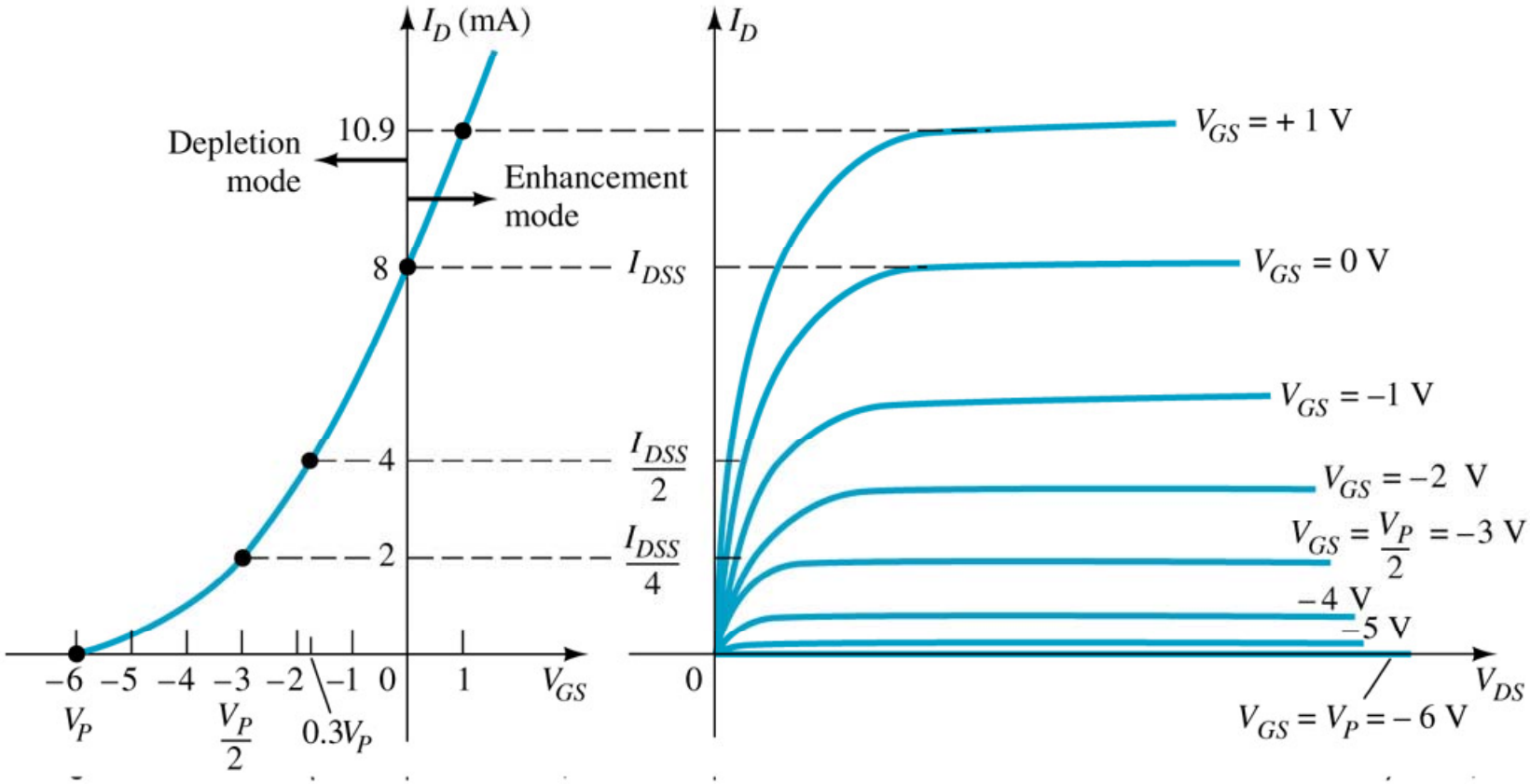
Depletion-Type MOSFET Construction



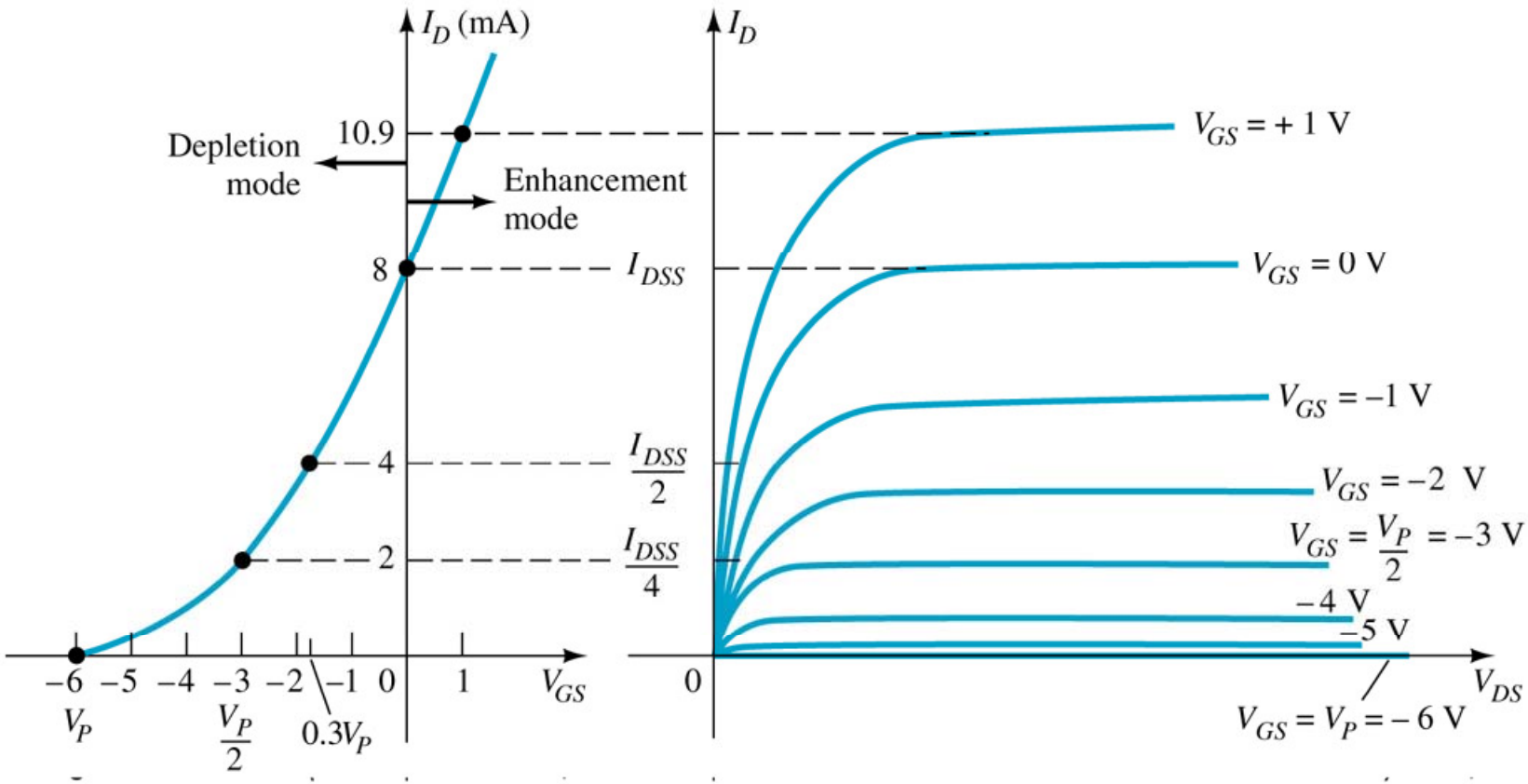
The Drain (D) and Source (S) connect to the to n-doped regions. These N-doped regions are connected via an n-channel. This n-channel is connected to the Gate (G) via a thin insulating layer of SiO_2. The n-doped material lies on a p-doped substrate that may have an additional terminal connection called SS.

Basic Operation

A Depletion MOSFET can operate in two modes: Depletion or Enhancement mode.



Depletion-type MOSFET in Depletion Mode



Depletion mode

The characteristics are similar to the JFET.

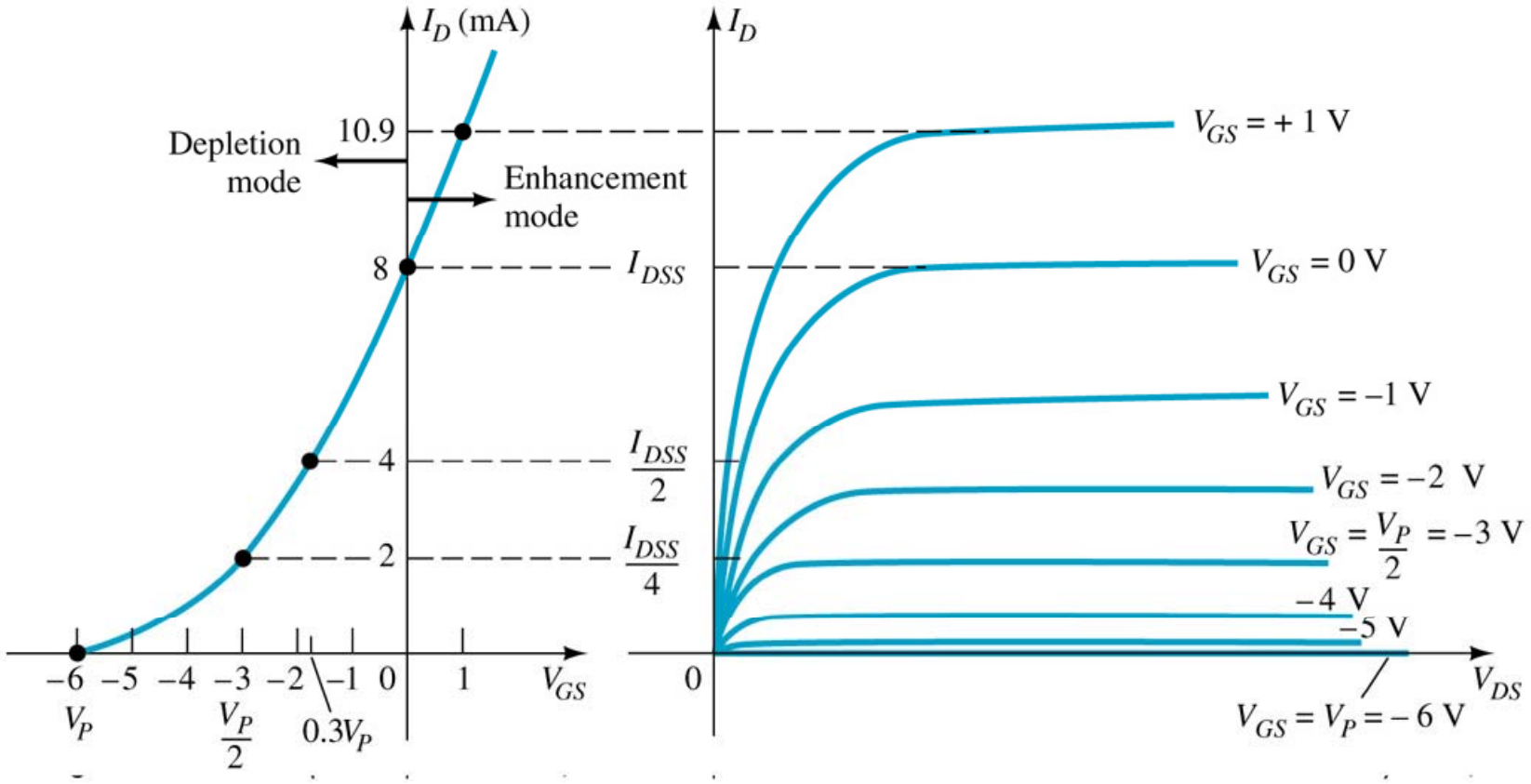
When $V_{GS} = 0V$, $I_D = I_{DSS}$

When $V_{GS} < 0V$, $I_D < I_{DSS}$

The formula used to plot the Transfer Curve still applies:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Depletion-type MOSFET in Enhancement Mode



Enhancement mode

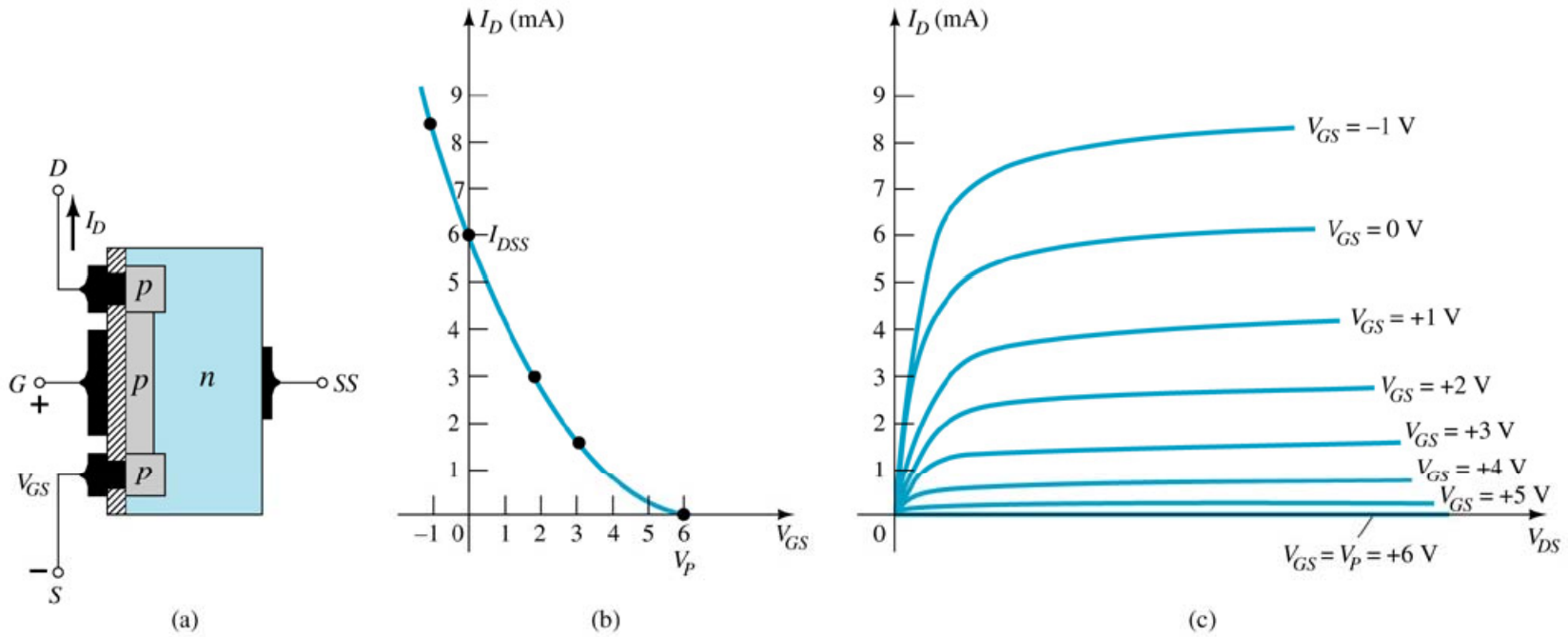
V_{GS} > 0V, I_D increases above I_{DSS}

The formula used to plot the Transfer Curve still applies:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

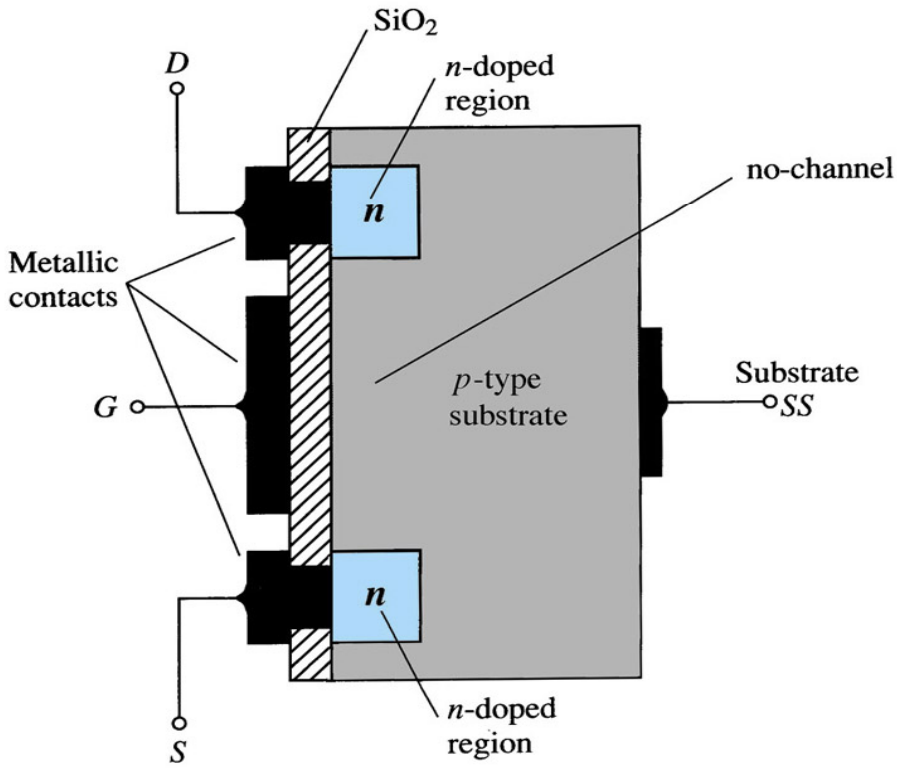
(note that VGS is now a positive polarity)

p-Channel Depletion-Type MOSFET



The p-channel Depletion-type MOSFET is similar to the n-channel except that the voltage polarities and current directions are reversed.

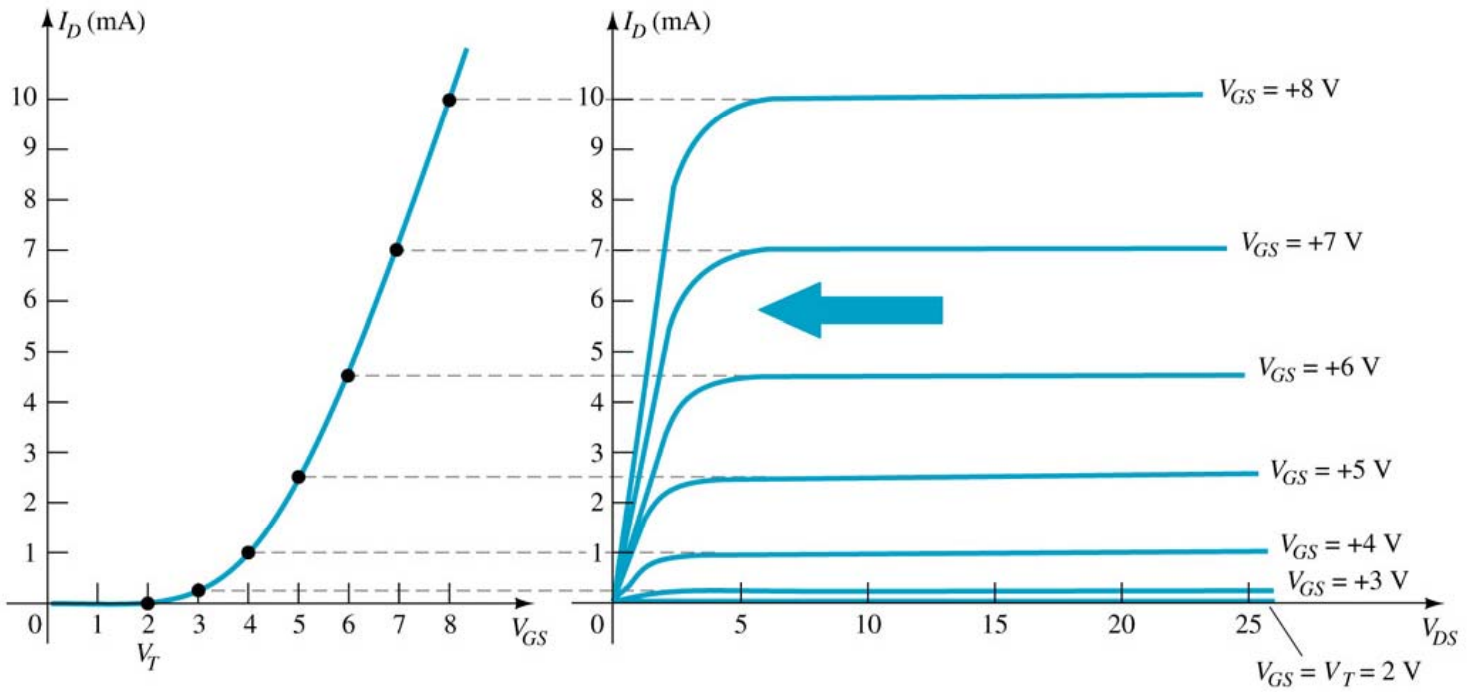
Enhancement-Type MOSFET Construction



The Drain (D) and Source (S) connect to the to n-doped regions. These n-doped regions are connected via an n-channel. The Gate (G) connects to the p-doped substrate via a thin insulating layer of SiO_2. There is no channel. The n-doped material lies on a p-doped substrate that may have an additional terminal connection called SS.

Basic Operation

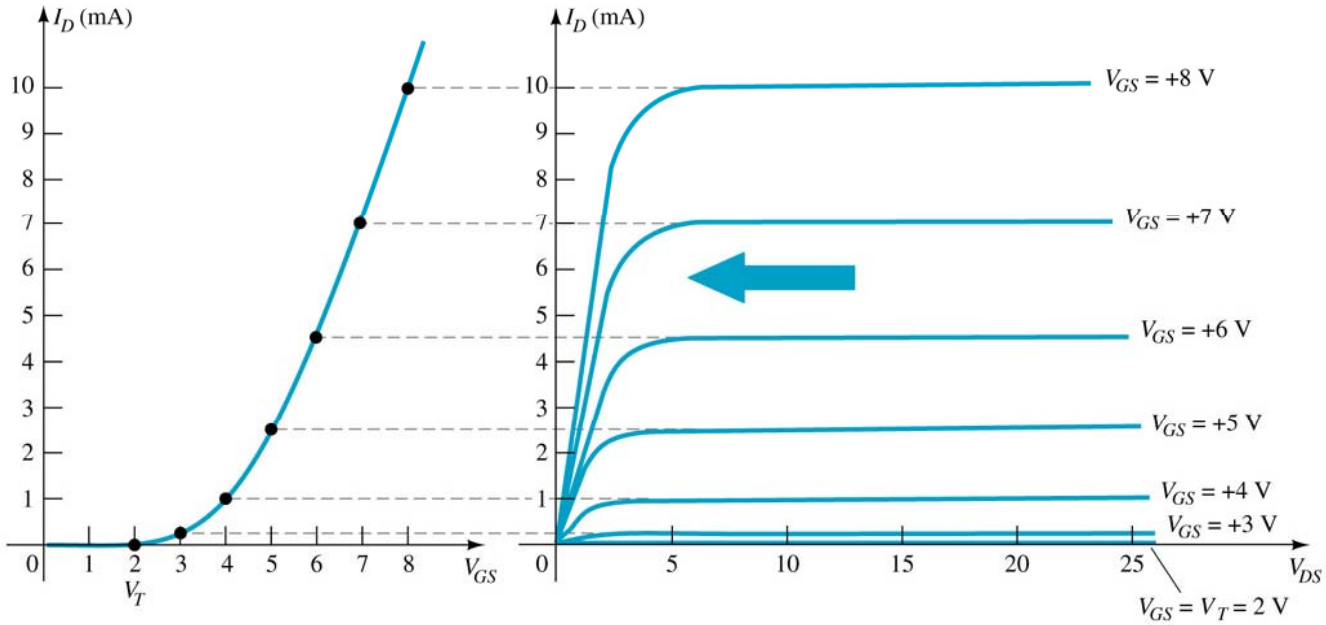
The Enhancement-type MOSFET only operates in the enhancement mode.



$$V_{Dsat} = V_{GS} - V_T$$

V_{GS} is always positive
As V_{GS} increases, I_D increases
But if V_{GS} is kept constant and V_{DS} is increased, then I_D saturates (I_{DSS})
The saturation level, V_{DSsat} is reached.

Transfer Curve



$$I_D = k(V_{GS} - V_T)^2$$

To determine I_D given V_{GS}:

where V_T = threshold voltage or voltage at which the MOSFET turns on.

$$k = \frac{I_{D(on)}}{(V_{GS(ON)} - V_T)^2}$$

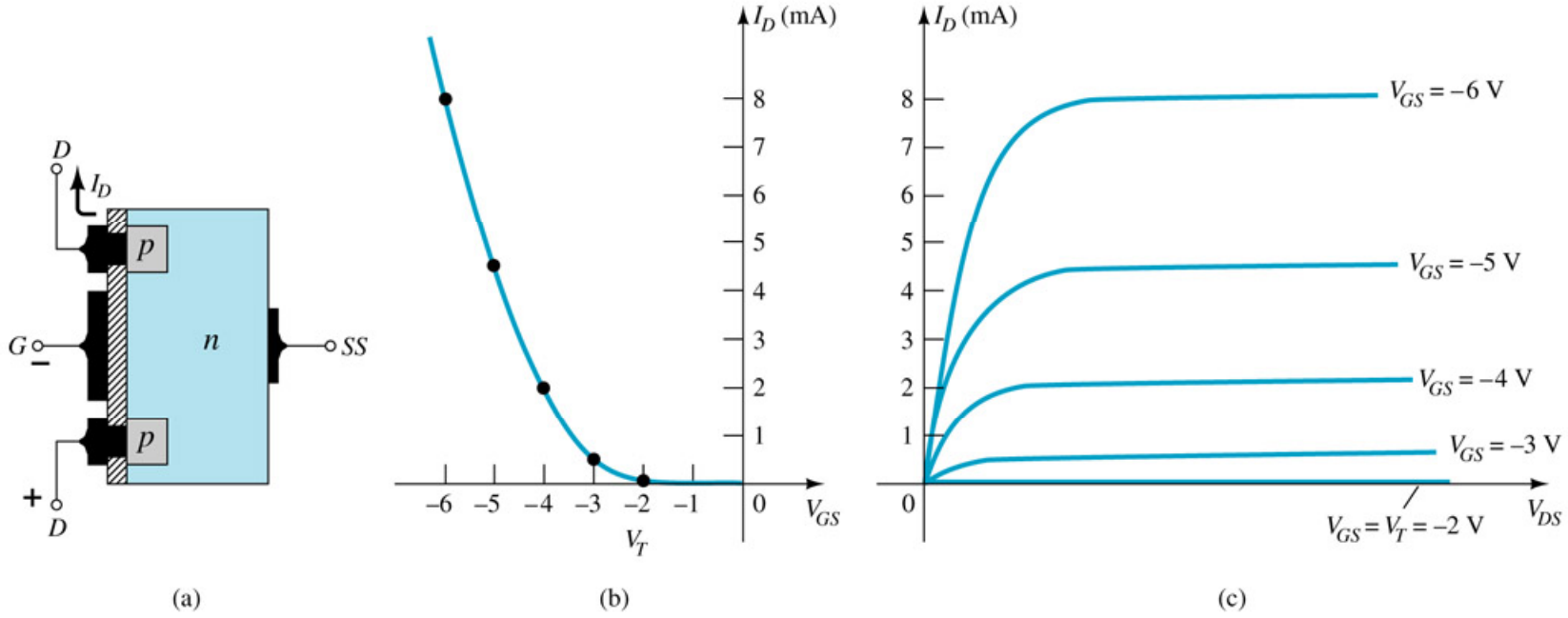
k = constant found in the specification sheet

k can also be determined by using values at a specific point and the formula:

$$V_{Dsat} = V_{GS} - V_T$$

p-Channel Enhancement-Type MOSFETs

The p-channel Enhancement-type MOSFET is similar to the n-channel except that the voltage polarities and current directions a



MOSFET Handling

MOSFETs are very static sensitive. Because of the very thin SiO_2 layer between the external terminals and the layers of the device, any small electrical discharge can stablish an unwanted conduction.

Protection:

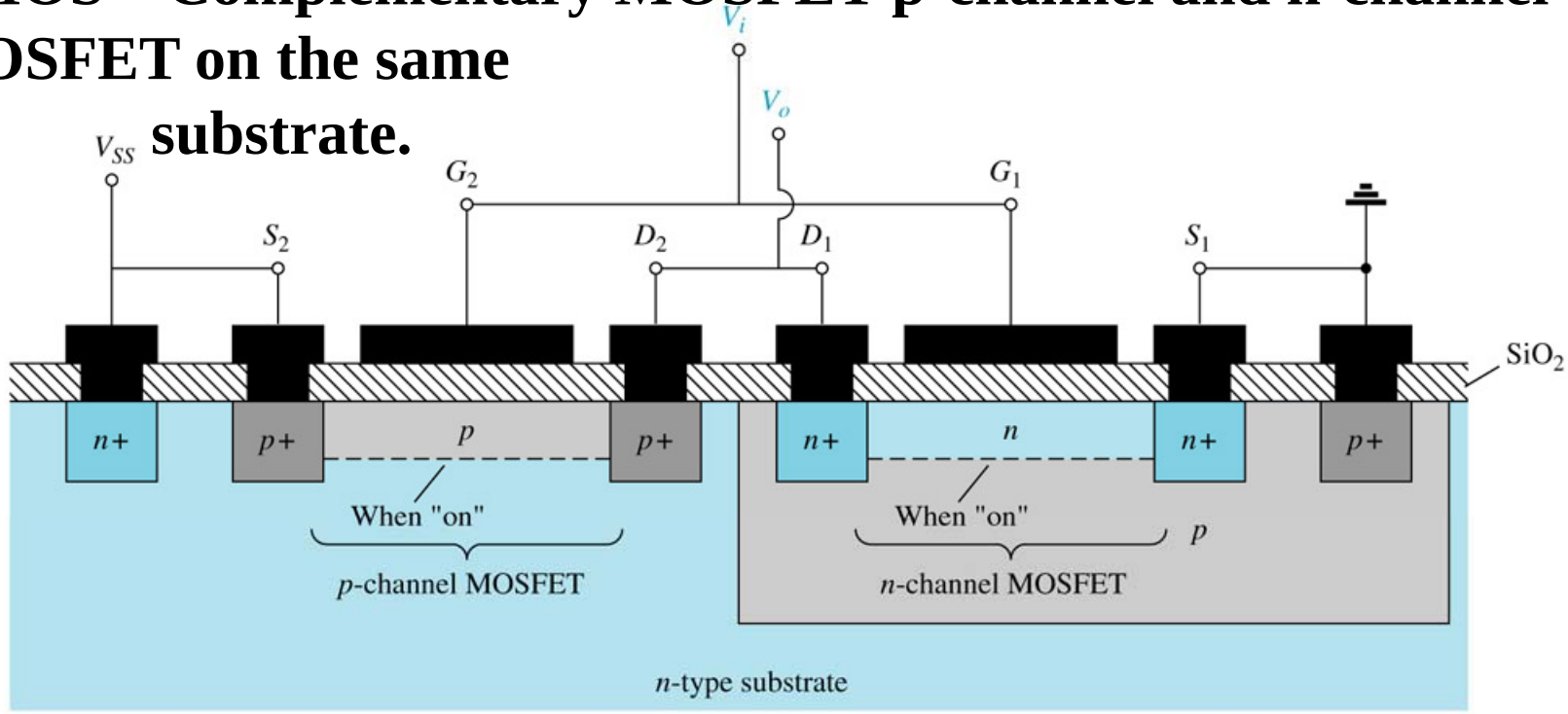
•Always transport in a static sensitive bag

•Always wear a static strap when handling MOSFETS

• Apply voltage limiting devices between the Gate and Source, such as back-to-back Zeners to limit any transient voltage.

CMOS

CMOS – Complementary MOSFET p-channel and n-channel MOSFET on the same substrate.

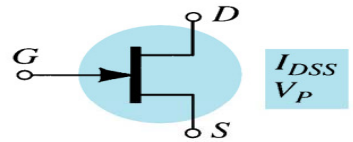


Advantage:

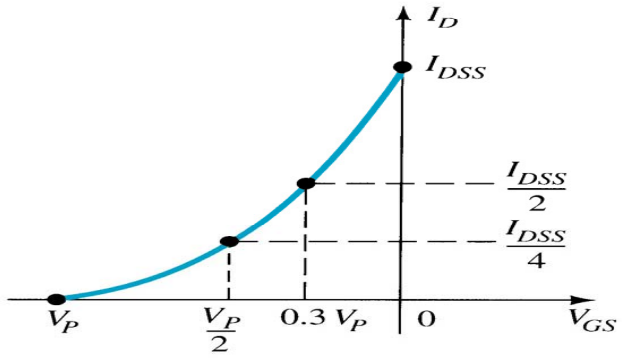
- **Useful in logic circuit designs**
- **Higher input impedance**
- **Faster switching speeds**
- **Lower operating power levels**

Summary Table

$I_G = 0$ A, $I_D = I_S$



$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$



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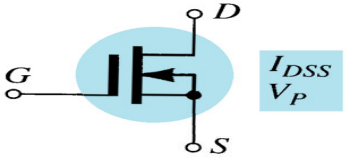

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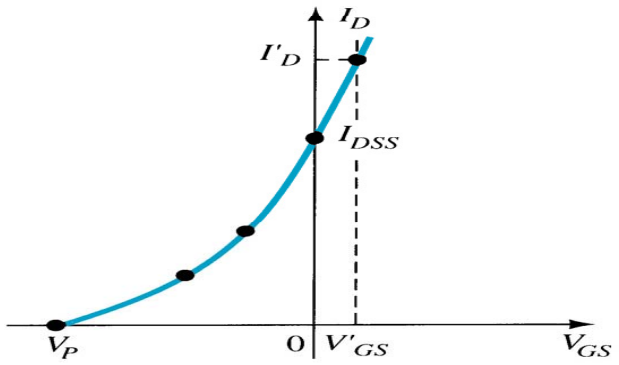

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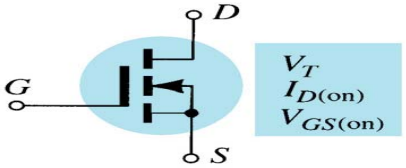
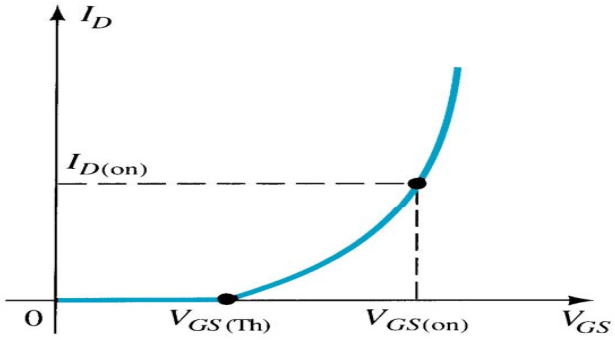


$$I_D = k(\ _{GS} - V_{GS\,(Th)})^2$$

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS\,(Th)})^2}$$



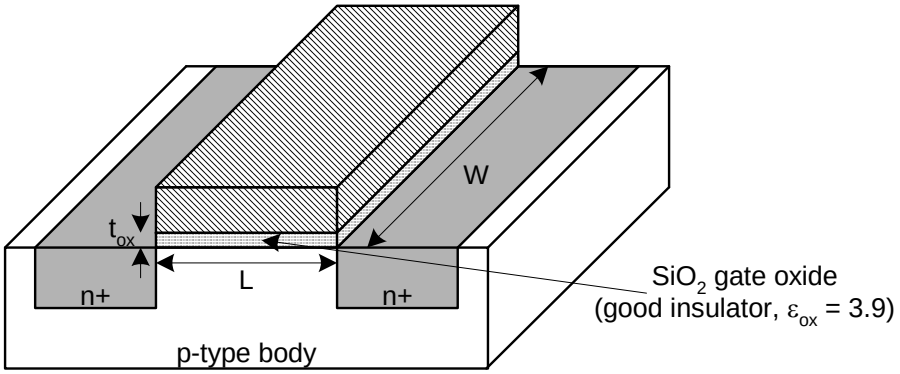
- So far, we have treated transistors as ideal switches
- An ON transistor passes a finite amount of current
  - Depends on terminal voltages
  - Derive current-voltage (I-V) relationships
- Transistor gate, source, drain all have capacitance
  - $I = C (\Delta V/\Delta t) \rightarrow \Delta t = (C/I)\, \Delta V$
  - Capacitance and current determine speed
- Also explore what a “degraded level” really means

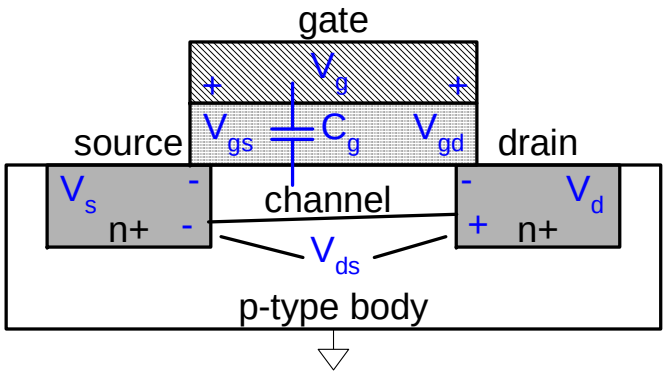
I-V Characteristics

- In Linear region, I_{ds} depends on
  - How much charge is in the channel?
  - How fast is the charge moving?

Channel Charge

- MOS structure looks like parallel plate capacitor while operating in inversion
  - Gate – oxide – channel
- $Q_{channel}$ =





Channel Charge

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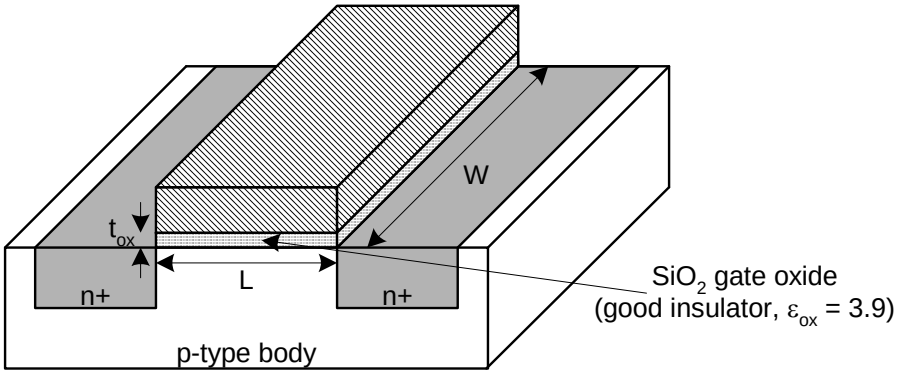
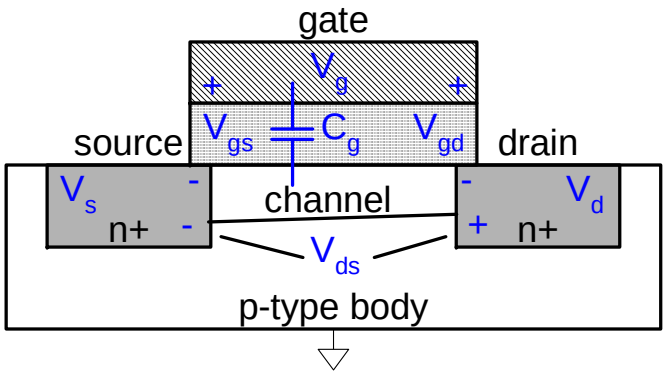
- $Q_{channel} = CV$
- C =

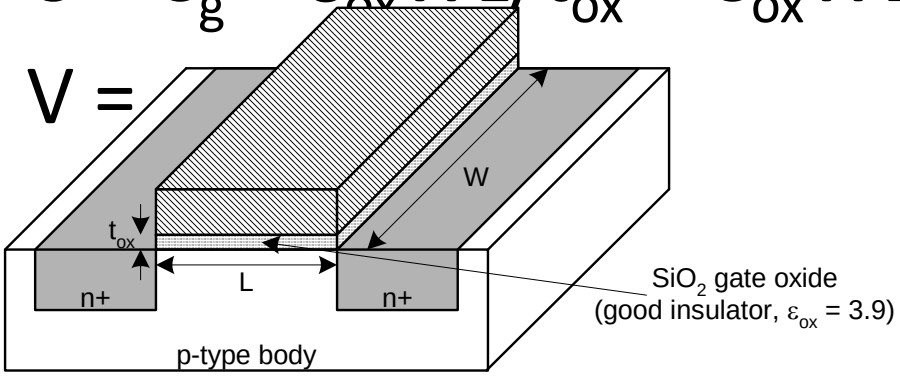


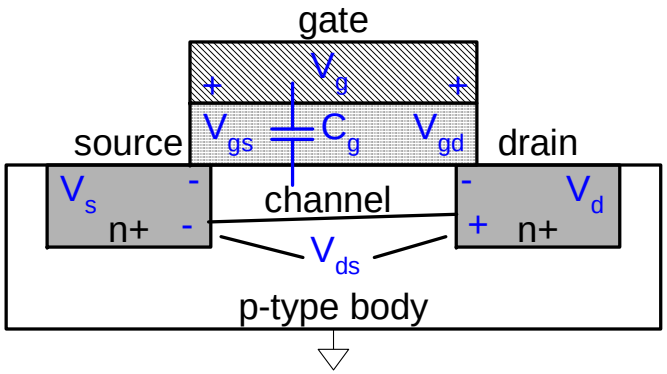


Channel Charge

- MOS structure looks like parallel plate capacitor while operating in inversion
  - Gate – oxide – channel
- $Q_{channel} = CV$
- $C = C_g = \varepsilon_{ox} WL/t_{ox} = C_{ox} WL$
- $V =$

$C_{ox} = \varepsilon_{ox} / t_{ox}$





Channel Charge

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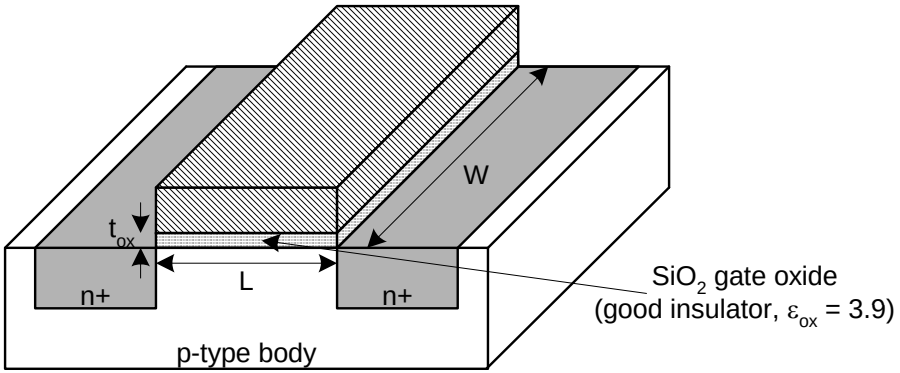
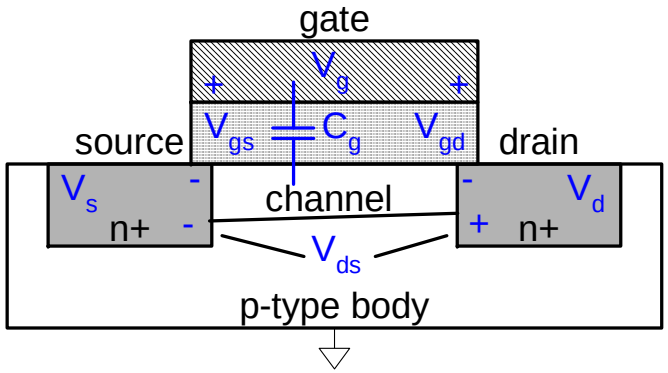
  - Gate – oxide – channel
- $Q_{channel} = CV$
- $C = C_g = \varepsilon_{ox} WL/t_{ox} = C_{ox} WL$
- $V = V_{gc} - V_t = (V_{gs} - V_{ds}/2) - V_t$

$C_{ox} = \varepsilon_{ox} / t_{ox}$





Carrier velocity

- Charge is carried by e-
- Carrier velocity *v* proportional to lateral E-field between source and drain
- *v* =

Carrier velocity

- Charge is carried by e-
- Carrier velocity *v* proportional to lateral E-field between source and drain
- $v = \mu E$ μ called mobility
- E =

Carrier velocity

- Charge is carried by e-
- Carrier velocity *v* proportional to lateral E-field between source and drain
- $v = \mu E$ μ called mobility
- $E = V_{ds}/L$
- Time for carrier to cross channel:
  - $t =$

Carrier velocity

- Charge is carried by e-
- Carrier velocity *v* proportional to lateral E-field between source and drain
- $v = \mu E$ μ called mobility
- $E = V_{ds}/L$
- Time for carrier to cross channel:
  - $t = L / v$

nMOS Linear I-V

- Now we know
  - How much charge $Q_{channel}$ is in the channel
  - How much time *t* each carrier takes to cross

$I_{ds} =$

nMOS Linear I-V

- Now we know
  - How much charge $Q_{channel}$ is in the channel
  - How much time *t* each carrier takes to cross

$$I_{ds} = \frac{Q_{\text{channel}}}{t}$$

$$=$$

nMOS Linear I-V

- Now we know
  - How much charge $Q_{channel}$ is in the channel
  - How much time *t* each carrier takes to cross

$$I_{ds} = \frac{Q_{\text{channel}}}{t}$$

$$= \mu C_{\text{ox}} \frac{W}{L}\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds}$$

$$= \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds}$$

$$\beta = \mu C_{\text{ox}} \frac{W}{L}$$

nMOS Saturation I-V

- If $V_{gd} < V_t$, channel pinches off near drain
  - When $V_{ds} > V_{dsat} = V_{gs} - V_t$
- Now drain voltage no longer increases current

$$I_{ds} =$$

nMOS Saturation I-V

- If $V_{gd} < V_t$, channel pinches off near drain
  - When $V_{ds} > V_{dsat} = V_{gs} - V_t$
- Now drain voltage no longer increases current

$$I_{ds} = \beta\left(V_{gs} - V_t - V_{dsat}/2\right)V_{dsat}$$

nMOS Saturation I-V

- If $V_{gd} < V_t$, channel pinches off near drain
  - When $V_{ds} > V_{dsat} = V_{gs} - V_t$
- Now drain voltage no longer increases current

$$I_{ds} = \beta\left(V_{gs} - V_t - V_{dsat}/2\right)V_{dsat}$$

$$= \frac{\beta}{2}\left(V_{gs} - V_t\right)^2$$

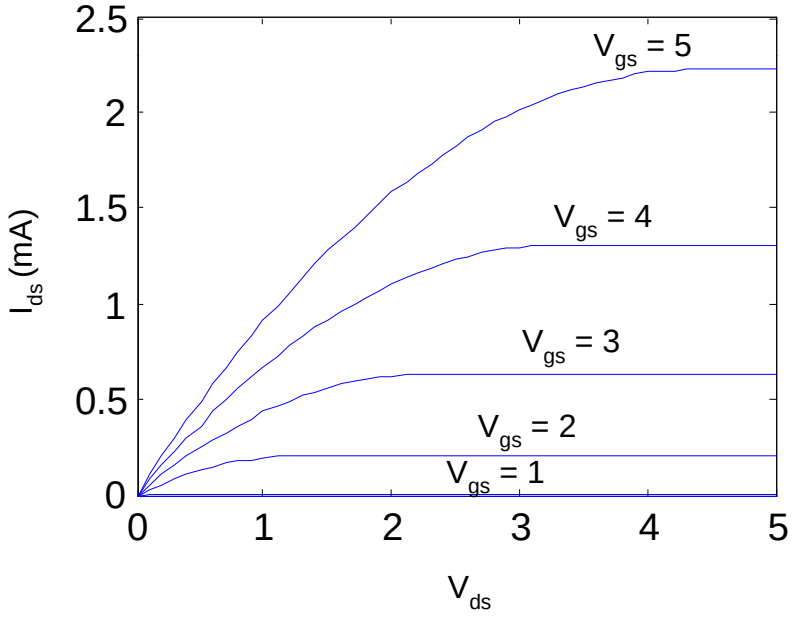
nMOS I-V Summary

- *Shockley* 1st order transistor models

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds} & V_{ds} < V_{dsat} \quad \text{linear} \\ \frac{\beta}{2}\left(V_{gs} - V_t\right)^2 & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

Example

- Example: a 0.6 μm process from AMI semiconductor
  - t_{ox} = 100 Å
  - μ = 350 $cm^2/V*s$
  - V_t = 0.7 V
- Plot I_{ds} vs. V_{ds}
  - V_{gs} = 0, 1, 2, 3, 4, 5
  - Use W/L = 4/2 λ



$$\beta = \mu C_{ox}\frac{W}{L} = (350)\left(\frac{3.9 \bullet 8.85\cdot 10^{-14}}{100\cdot 10^{-8}}\right)\left(\frac{W}{L}\right) = 120\frac{W}{L}\mu A/V^2$$

pMOS I-V

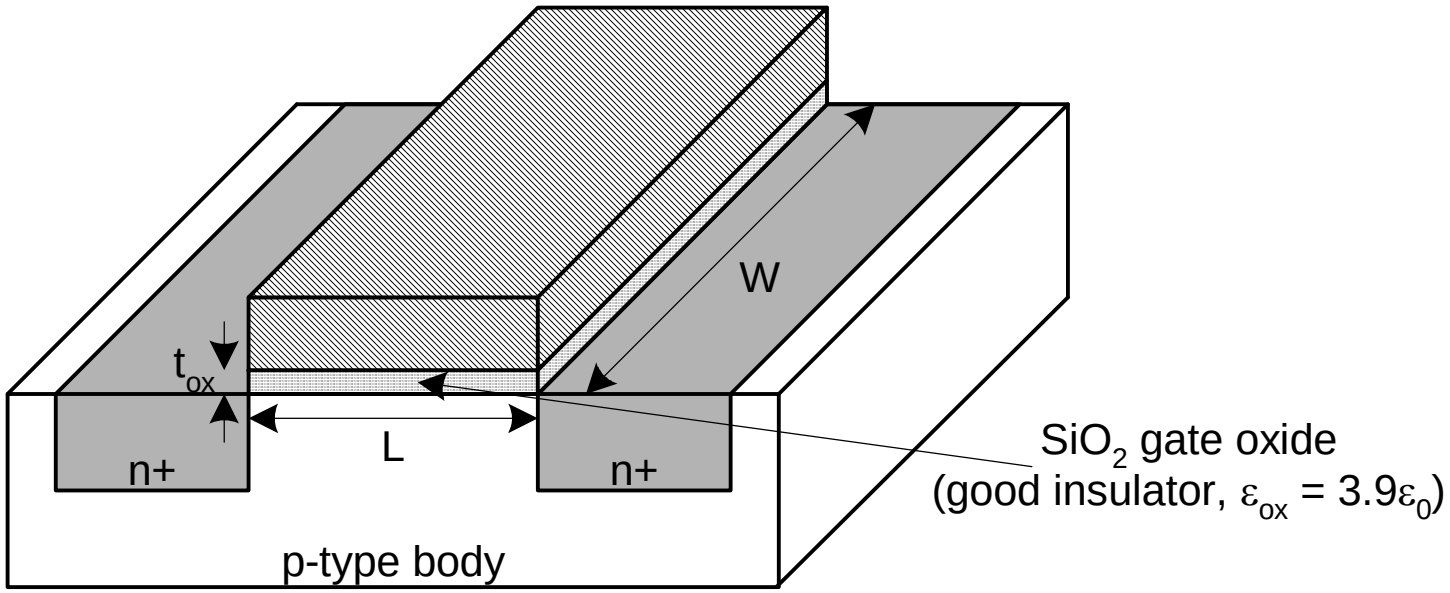
- All dopings and voltages are inverted for pMOS
- Mobility μ_p is determined by holes
  - Typically 2-3x lower than that of electrons μ_n
  - 120 $cm^2/V*s$ in AMI 0.6 μm process
- Thus pMOS must be wider to provide same current
  - In this class, assume $\mu_n / \mu_p = 2$

Capacitance

- Any two conductors separated by an insulator have capacitance
- Gate to channel capacitor is very important
  - Creates channel charge necessary for operation
- Source and drain have capacitance to body
  - Across reverse-biased diodes
  - Called diffusion capacitance because it is associated with source/drain diffusion

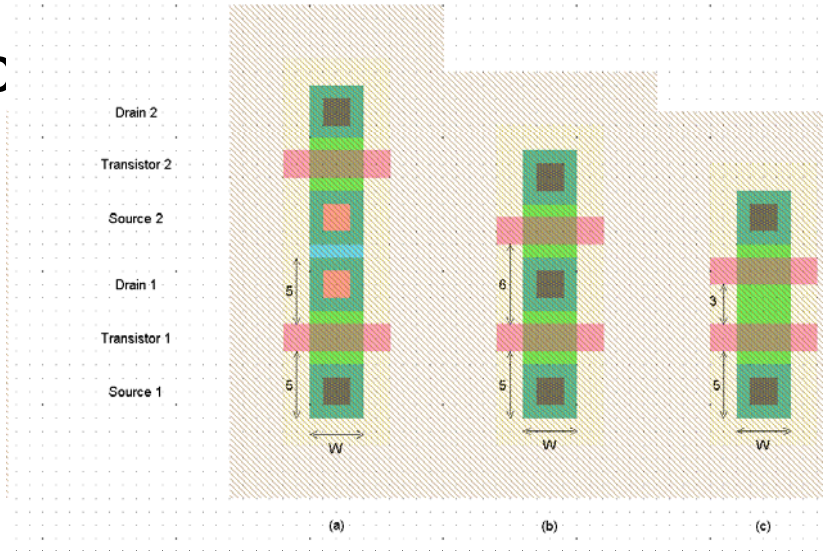
Gate Capacitance

- Approximate channel as connected to source
- $C_{gs} = \varepsilon_{ox}WL/t_{ox} = C_{ox}WL = C_{permicron}W$
- $C_{permicron}$ is typically about 2 fF/μm



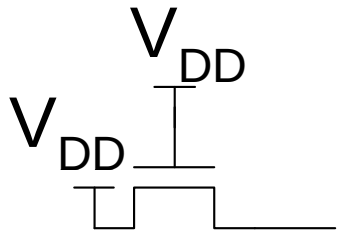
Diffusion Capacitance

- C_{sb}, C_{db}
- Undesirable, called *parasitic* capacitance
- Capacitance depends on area and perimeter
  - Use small diffusion nc
  - Comparable to C_g for contacted diff
  - ½ C_g for uncontacted
  - Varies with process



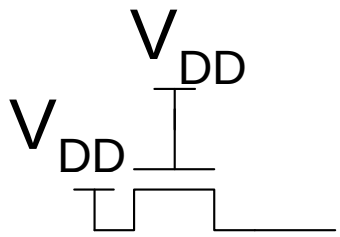
Pass Transistors

- We have assumed source is grounded
- What if source > 0?
  - e.g. pass transistor passing V_{DD}

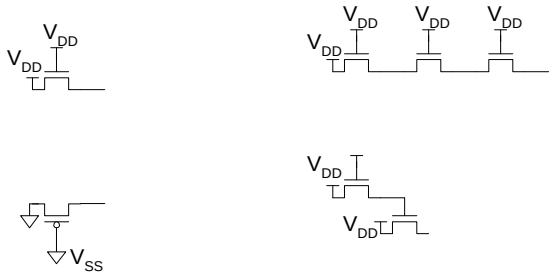


Pass Transistors

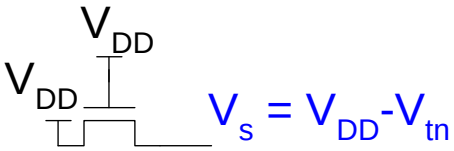
- We have assumed source is grounded
- What if source > 0?
  - e.g. pass transistor passing V_{DD}
- $V_g = V_{DD}$
  - If $V_s > V_{DD}-V_t$, $V_{gs} < V_t$
  - Hence transistor would turn itself off
- nMOS pass transistors pull no higher than $V_{DD}-V_{tn}$
  - Called a degraded "1"
  - Approach degraded value slowly (low I_{ds})
- pMOS pass transistors pull no lower than V_{tp}

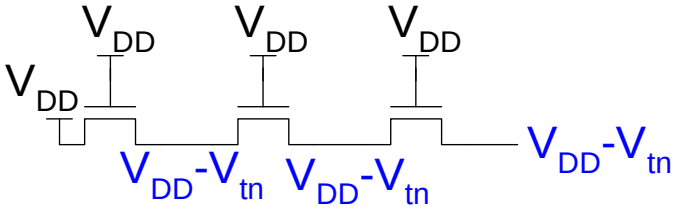


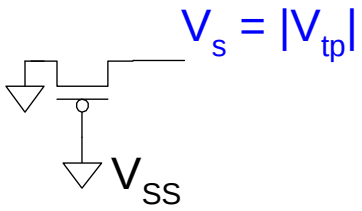
Pass Transistor Ckts

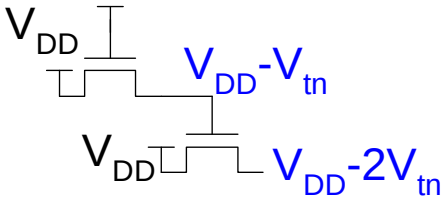


Pass Transistor Ckts







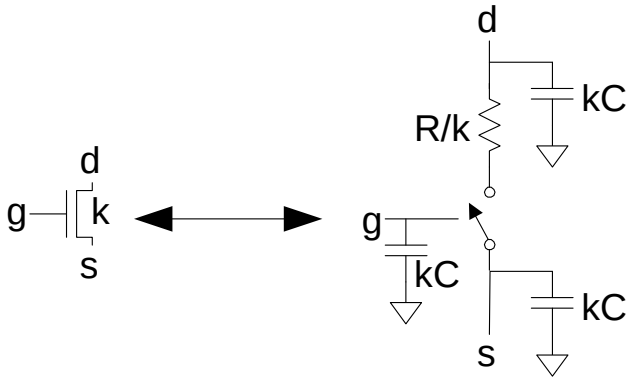


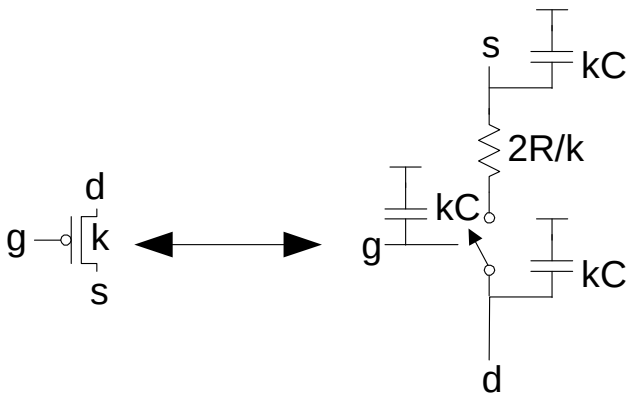
Effective Resistance

- Shockley models have limited value
  - Not accurate enough for modern transistors
  - Too complicated for much hand analysis
- Simplification: treat transistor as resistor
  - Replace $I_{ds}(V_{ds}, V_{gs})$ with effective resistance R
    - $I_{ds} = V_{ds}/R$
  - R averaged across switching of digital gate
- Too inaccurate to predict current at any given time
  - But good enough to predict RC delay

RC Delay Model

- Use equivalent circuits for MOS transistors
  - Ideal switch + capacitance and ON resistance
  - Unit nMOS has resistance R, capacitance C
  - Unit pMOS has resistance 2R, capacitance C
- Capacitance proportional to width
- Resistance inversely proportional to width



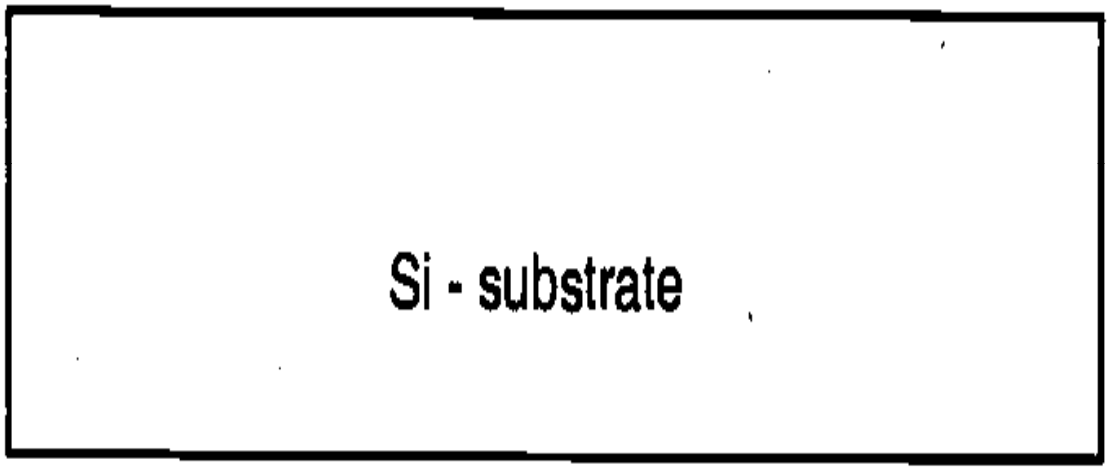


RC Values

- Capacitance
  - $C = C_g = C_s = C_d = 2$ fF/μm of gate width
  - Values similar across many processes
- Resistance
  - $R \approx 6$ KΩ*μm in 0.6um process
  - Improves with shorter channel lengths
- Unit transistors
  - May refer to minimum contacted device (4/2 λ)
  - Or maybe 1 μm wide device
  - Doesn't matter as long as you are consistent

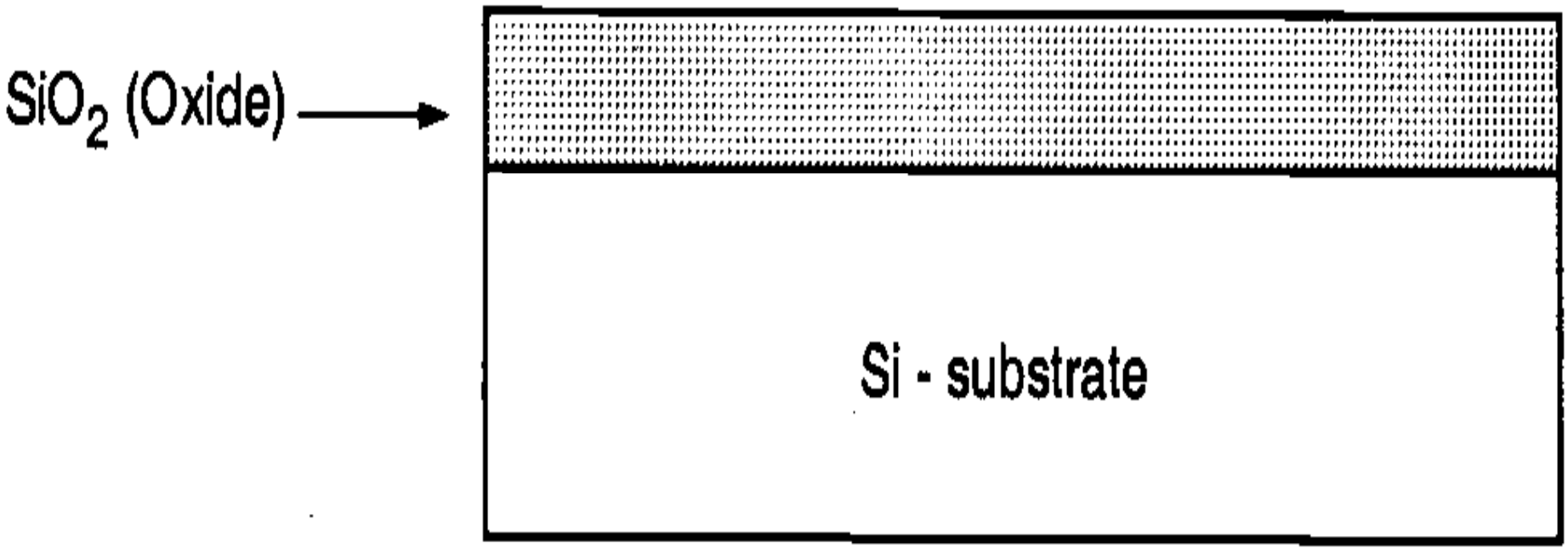
NMOS PROCESS

Fabrication of nmos

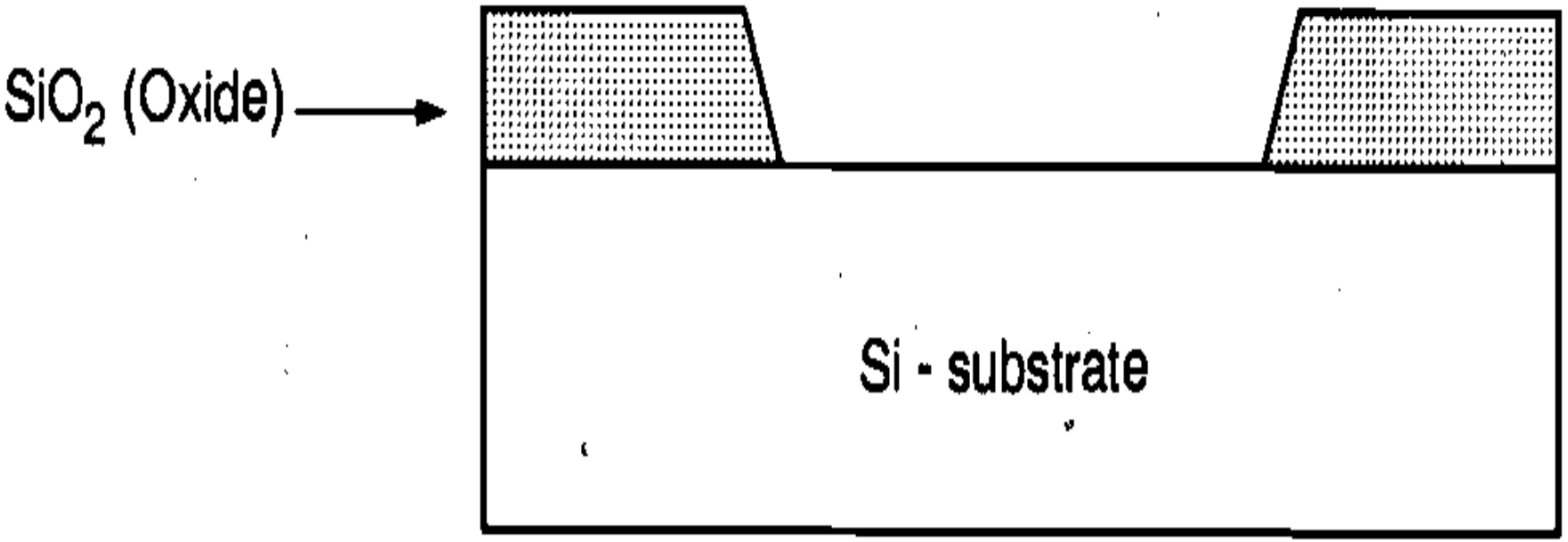


Processing is carried on single crystal silicon of high purity on which required P impurities are introduced as crystal is grown

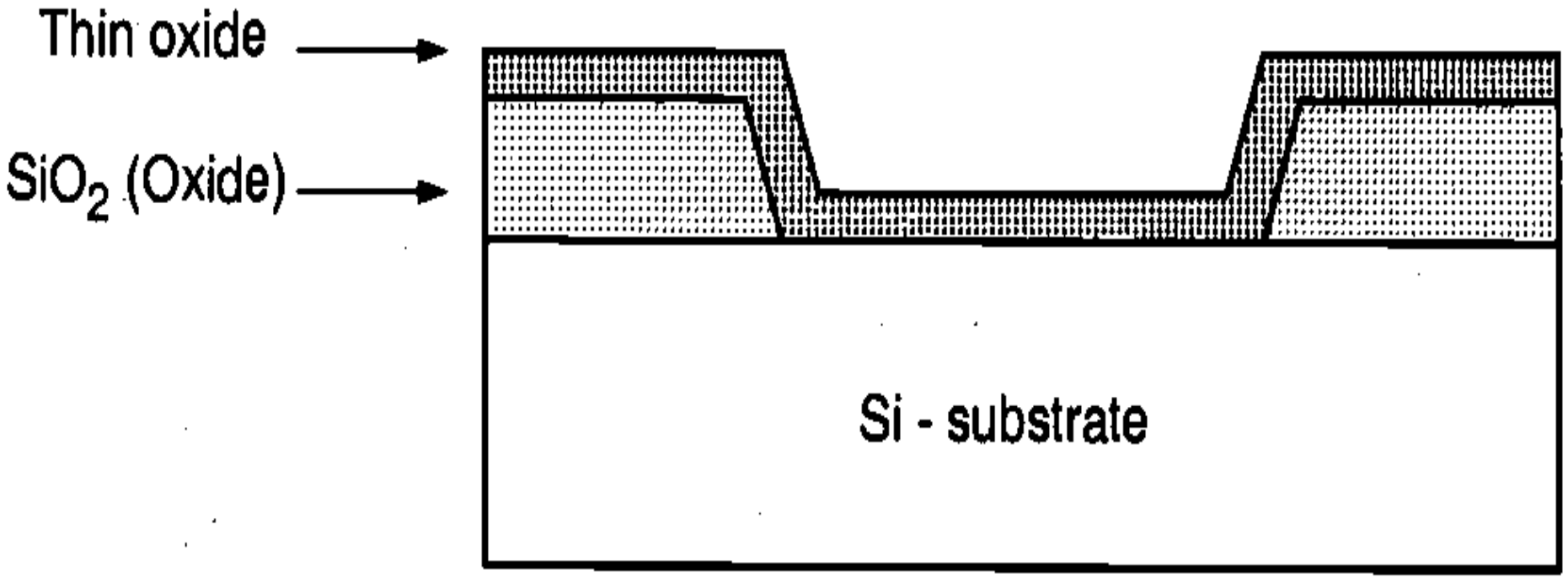
- Process start with the oxidation of the silicon substrate, in which a relatively thick silicon dioxide layer, also called field oxide, is created on the surface.



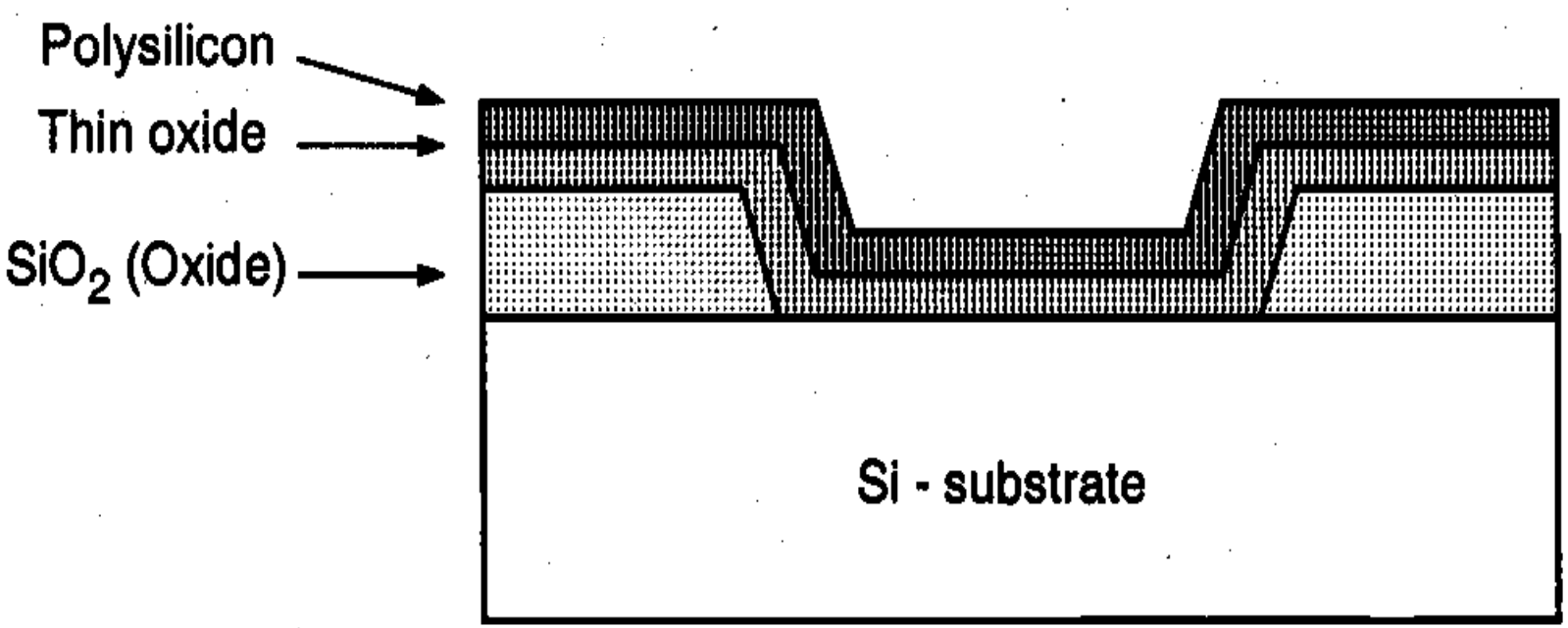
❑Then, the field oxide is selectivity etched to expose the silicon surface on which the MOS transistor will be created.



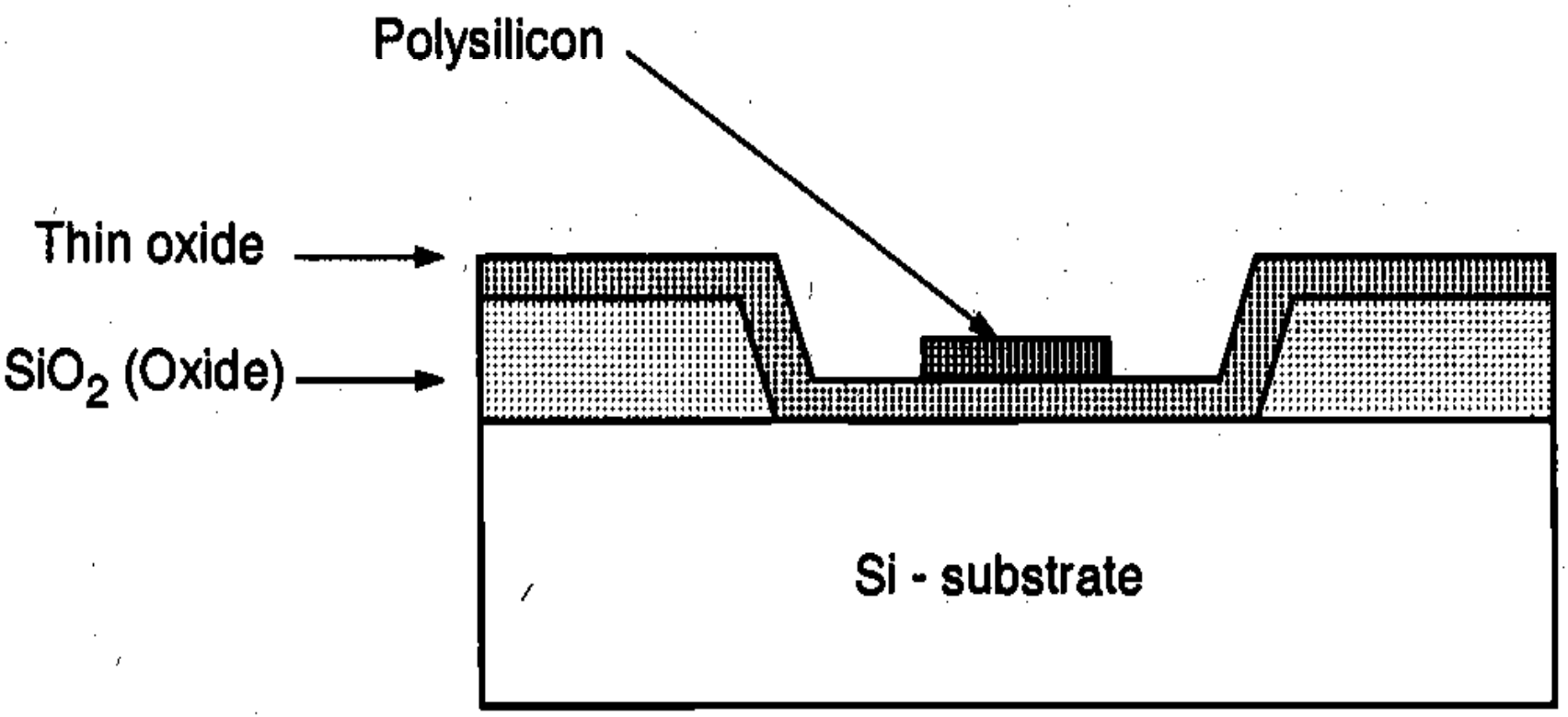
❑ The surface is covered with a thin, high-quality oxide layer, which will eventually form the gate oxide of the MOS transistor



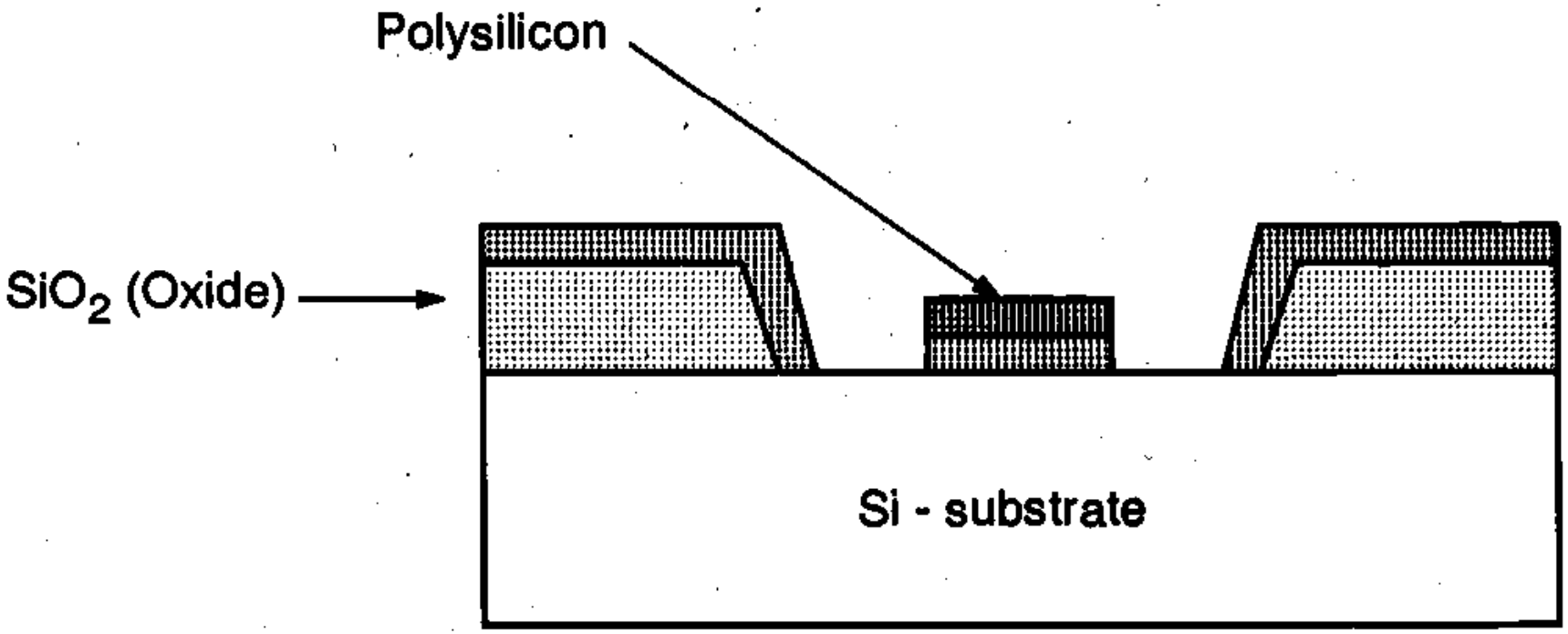
- On top of the thin oxide layer, a layer of polysilicon (Polycrystalline silicon) is deposited.
- Polysilicon is used both as gate electrode material for MOS transistors and also as an interconnect medium in silicon integrated circuits.
- Undoped polysilicon has relatively high resistivity.
- The resistivity of polysilicon can be reduced, however, by doping it with impurity atoms.



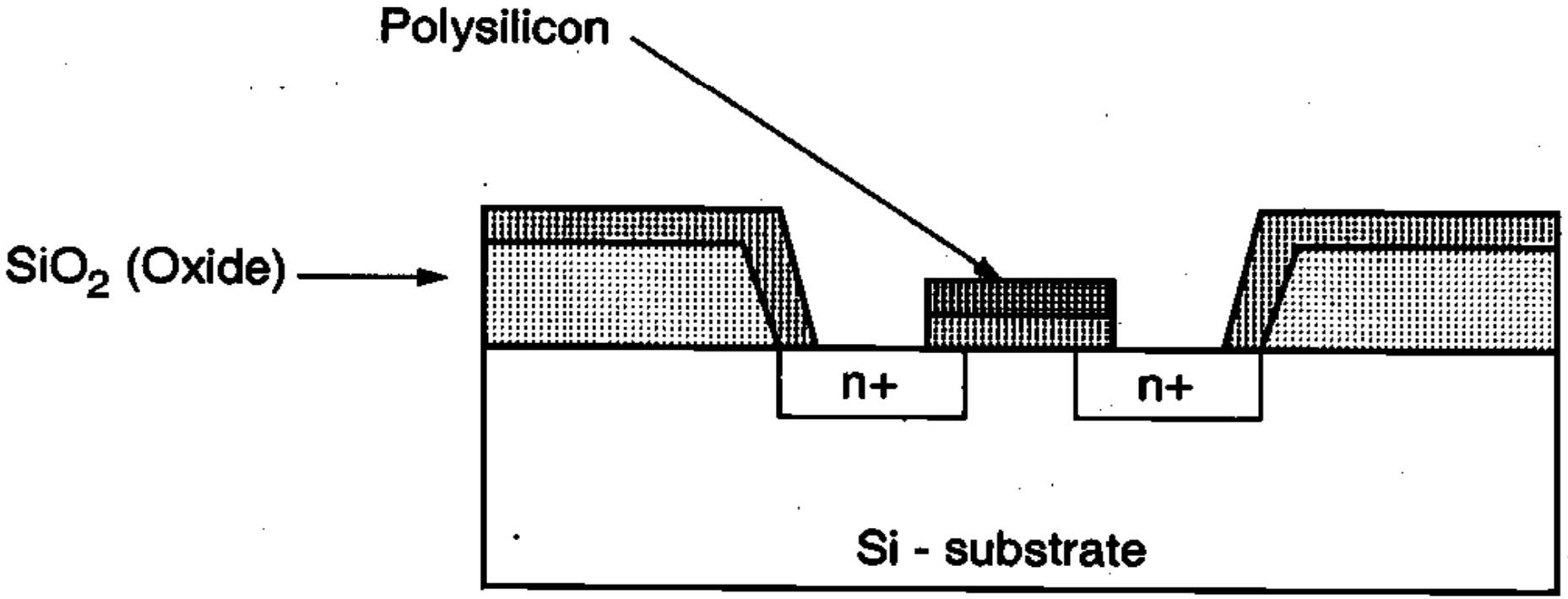
- After deposition, the polysilicon layer is patterned and etched to form the interconnects and the MOS transistor gates.



- The thin gate oxide not covered by polysilicon is also etched away, which exposes the base silicon surface on which the source and drain junctions are to be formed.

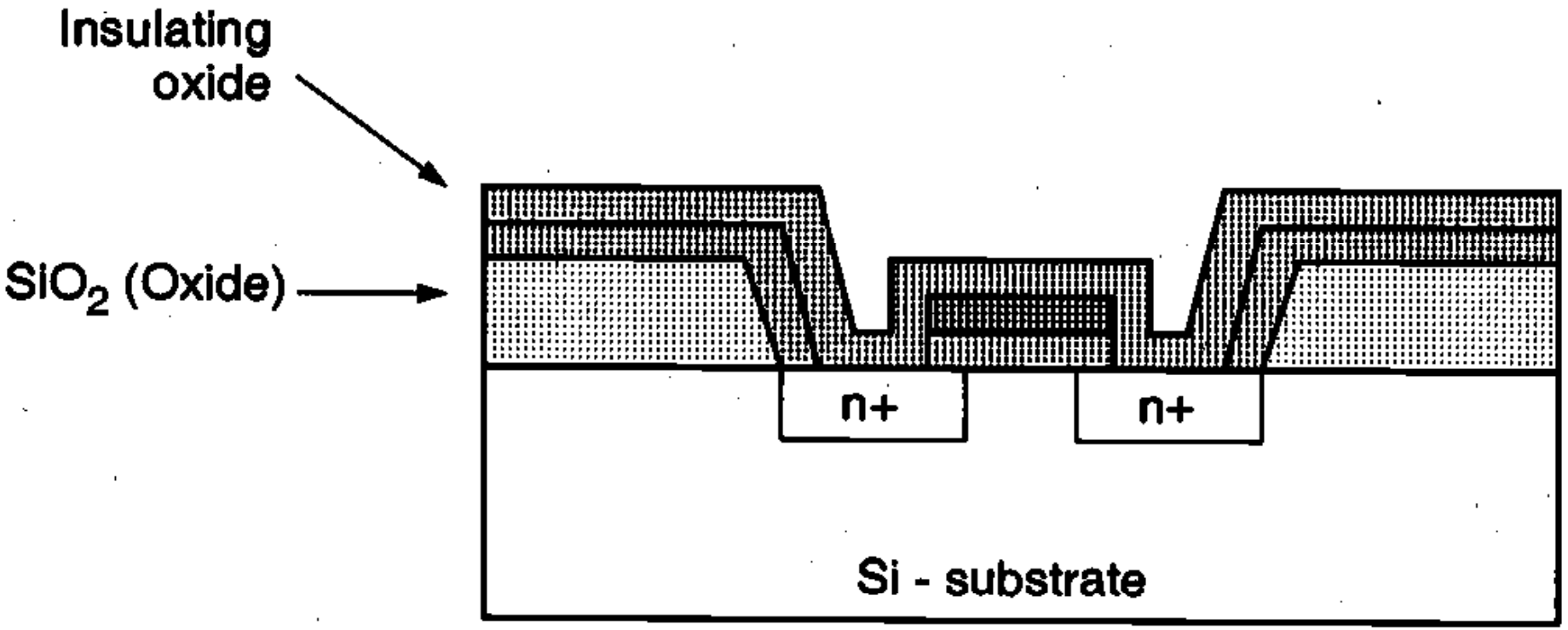


- The entire silicon surface is then doped with a high concentration of impurities, either through **diffusion or ion implantation**(in this case with donor atoms to produce n- type doping)
- This shows that the doping penetartes the exposed areas on the silicon surface, ultimately creating two n type regions(Source and drain junctions) in the p-type substrate.

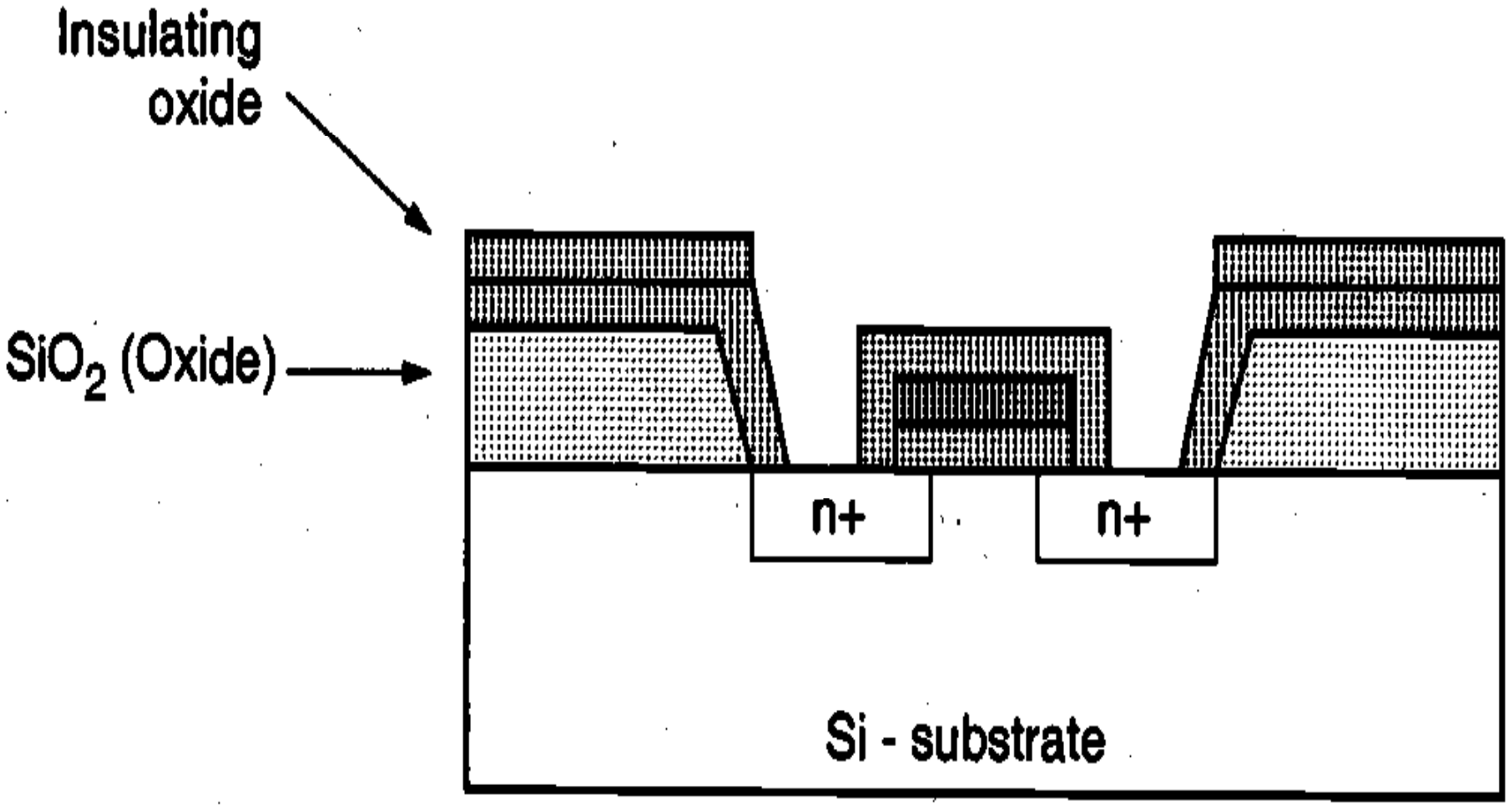


- The impurity doping also penetrates the polysilicon on the surface, reducing its resistivity.
- Polysilicon gate, which is patterned before doping, actually defines the precise location of the channel region and hence, the location of the source and the drain regions.
- This procedure allows very precise positioning of the two regions relative to the gate, it is also called the self-aligned process.

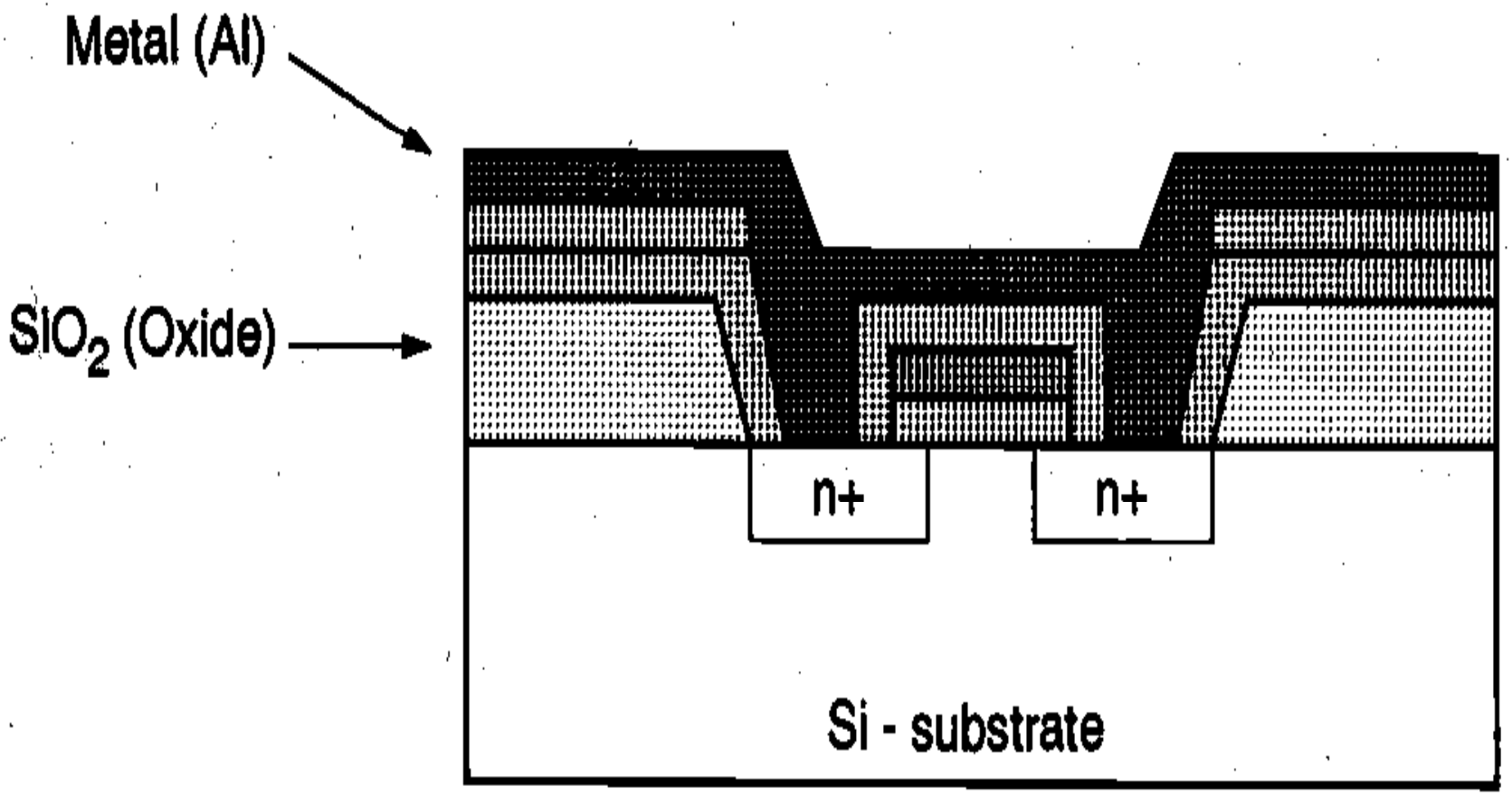
- Once the source and drain regions are completed, the entire surface is again covered with an insulating layer of silicon dioxide



❑ The insulating oxide layer is then patterned in order to provide contact windows for the drain and source junctions

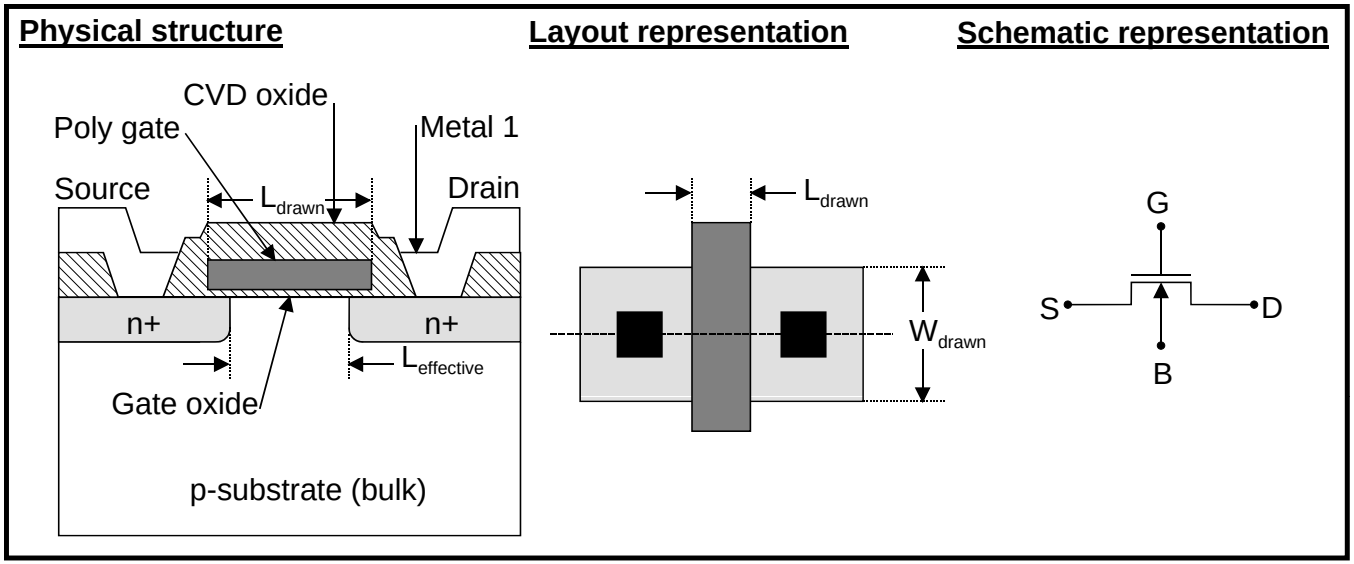


- The surface is covered with evaporated aluminum which will form the interconnects



CMOS PROCESS

Physical structure



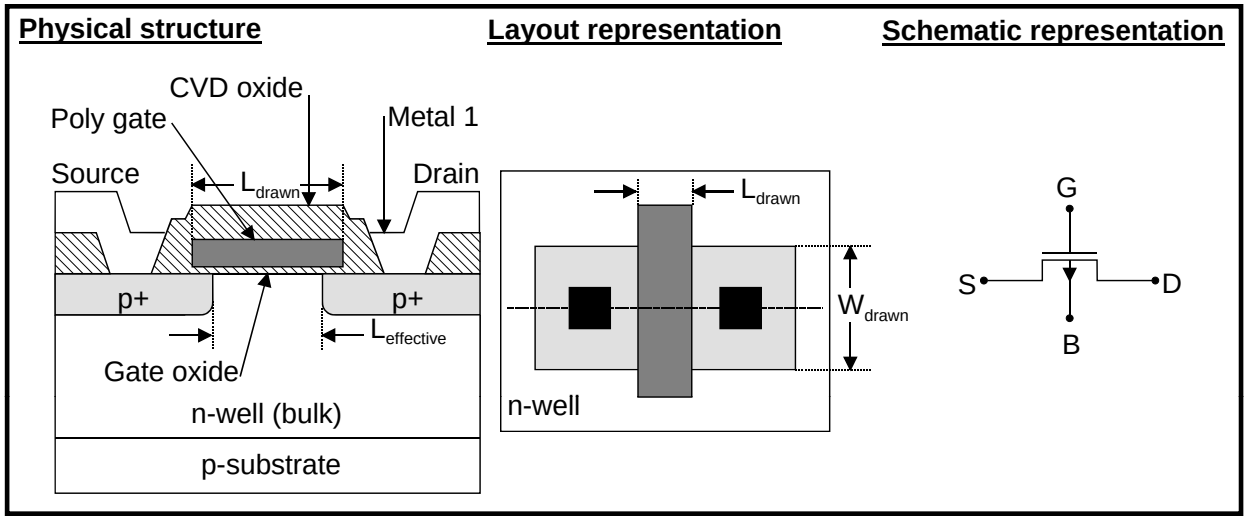
NMOS physical structure:

- p-substrate
- n+ source/drain
- gate oxide (SiO_2)
- polysilicon gate
- CVD oxide
- metal 1
- L_{eff}<L_{drawn} (lateral doping effects)

NMOS layout representation:

- Implicit layers:
  - oxide layers
  - substrate (bulk)
- Drawn layers:
  - n+ regions
  - polysilicon gate
  - oxide contact cuts
  - metal layers

Physical structure



PMOS physical structure:

- p-substrate
- n-well (bulk)
- p+ source/drain
- gate oxide (SiO_2)
- polysilicon gate
- CVD oxide
- metal 1

PMOS layout representation:

- Implicit layers:
  - oxide layers
- Drawn layers:
  - n-well (bulk)
  - n+ regions
  - polysilicon gate
  - oxide contact cuts
  - metal layers

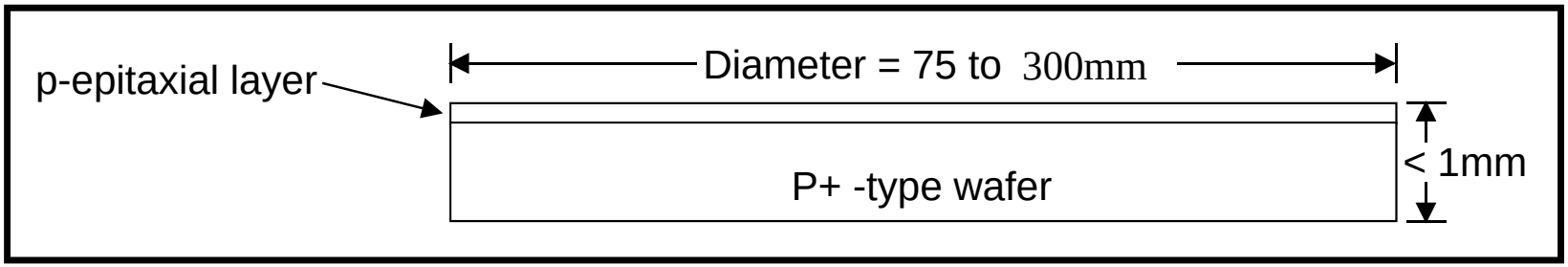
CMOS fabrication sequence

0. Start:

- For an n-well process the starting point is a p-type silicon wafer:
- wafer: typically 75 to 300mm in diameter and less than 1mm thick

1. Epitaxial growth:

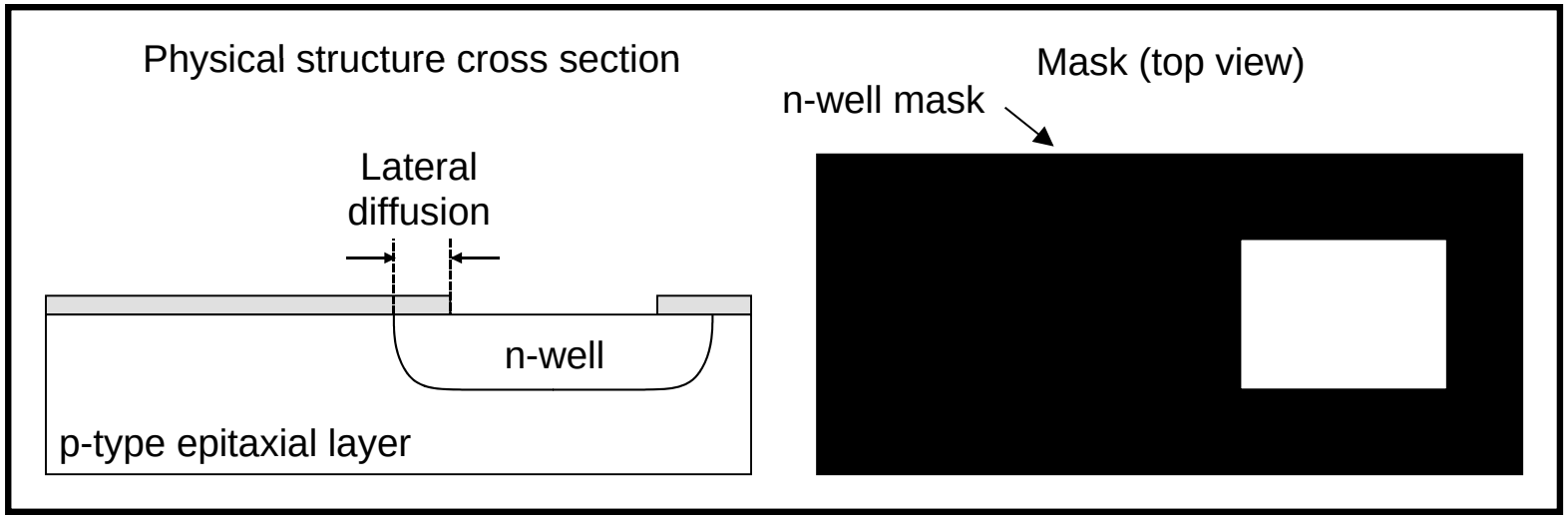
- A single p-type single crystal film is grown on the surface of the wafer by:
  - subjecting the wafer to high temperature and a source of dopant material
- The epi layer is used as the base layer to build the devices



CMOS fabrication sequence

2. N-well Formation:

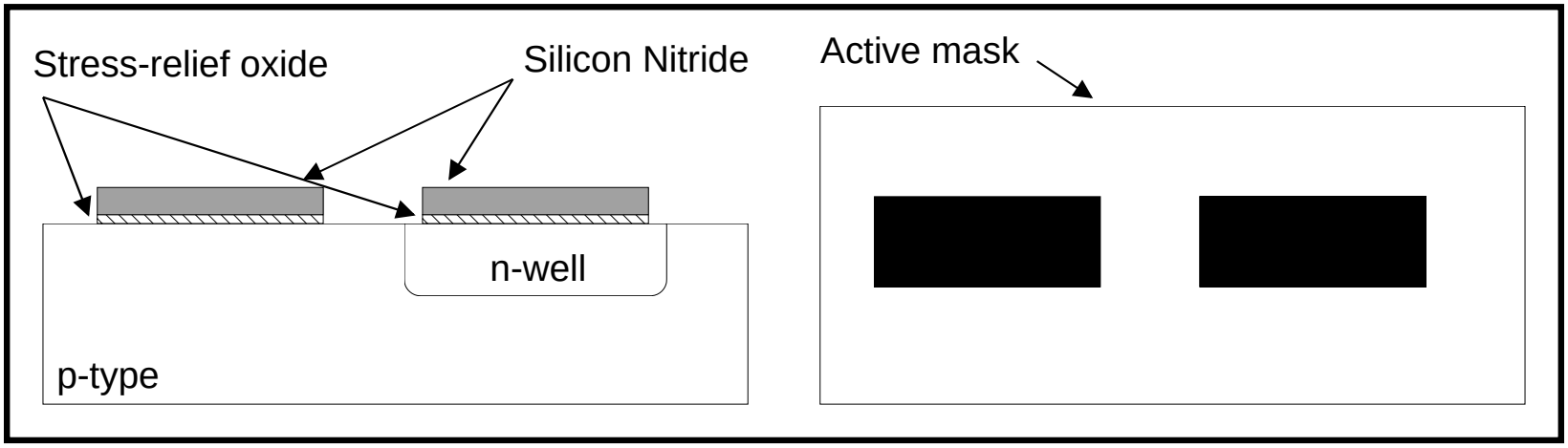
- PMOS transistors are fabricated in n-well regions
- The first mask defines the n-well regions
- N-well's are formed by ion implantation or deposition and diffusion
- Lateral diffusion limits the proximity between structures
- Ion implantation results in shallower wells compatible with today's fine-line processes



CMOS fabrication sequence

3. Active area definition:

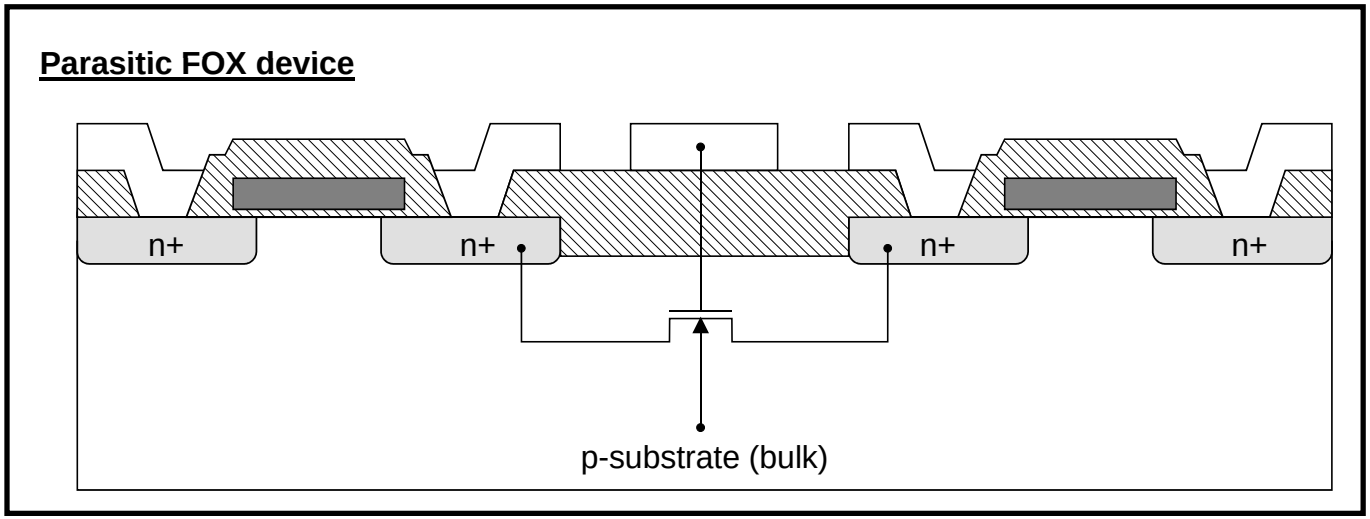
- Active area:
  - planar section of the surface where transistors are build
  - defines the gate region (thin oxide)
  - defines the n+ or p+ regions
- A thin layer of SiO_2 is grown over the active region and covered with silicon nitride



CMOS fabrication sequence

4. Isolation:

- Parasitic (unwanted) FET's exist between unrelated transistors (Field Oxide FET's)
- Source and drains are existing source and drains of wanted devices
- Gates are metal and polysilicon interconnects
- The threshold voltage of FOX FET's are higher than for normal FET's

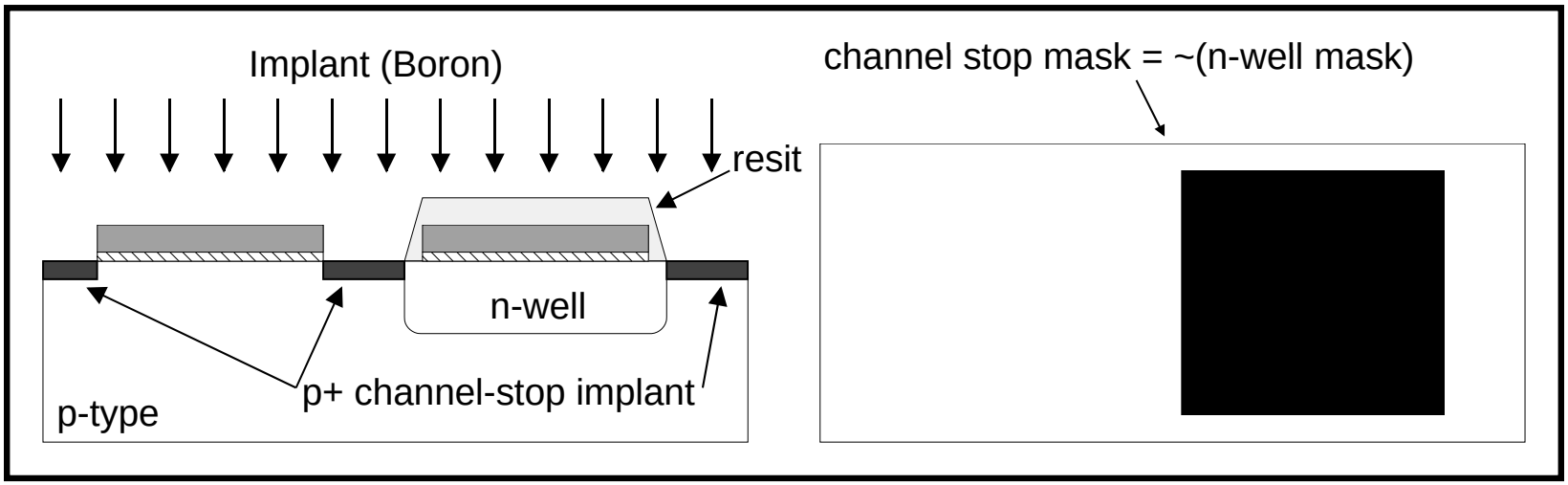


CMOS fabrication sequence

- FOX FET's threshold is made high by:
  - introducing a channel-stop diffusion that raises the impurity concentration in the substrate in areas where transistors are not required
  - making the FOX thick

4.1 Channel-stop implant

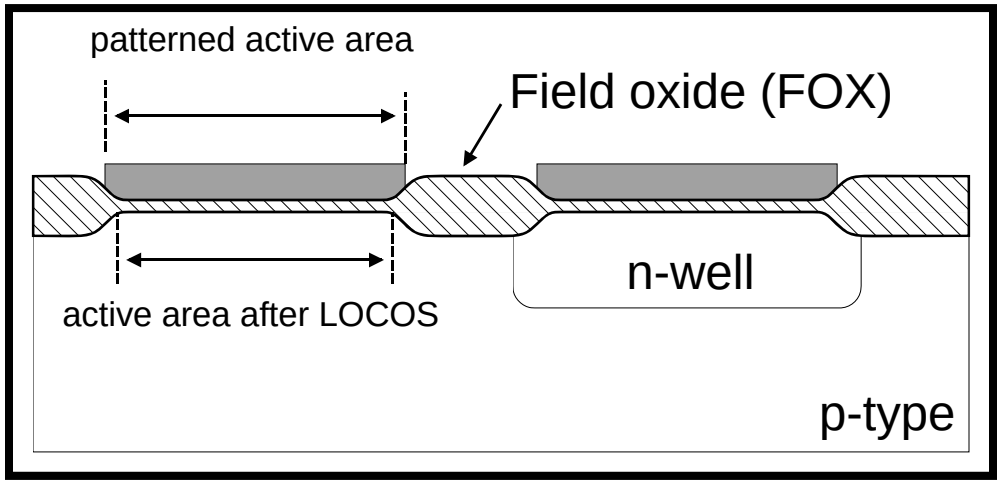
- The silicon nitride (over n-active) and the photoresist (over n-well) act as masks for the channel-stop implant



CMOS fabrication sequence

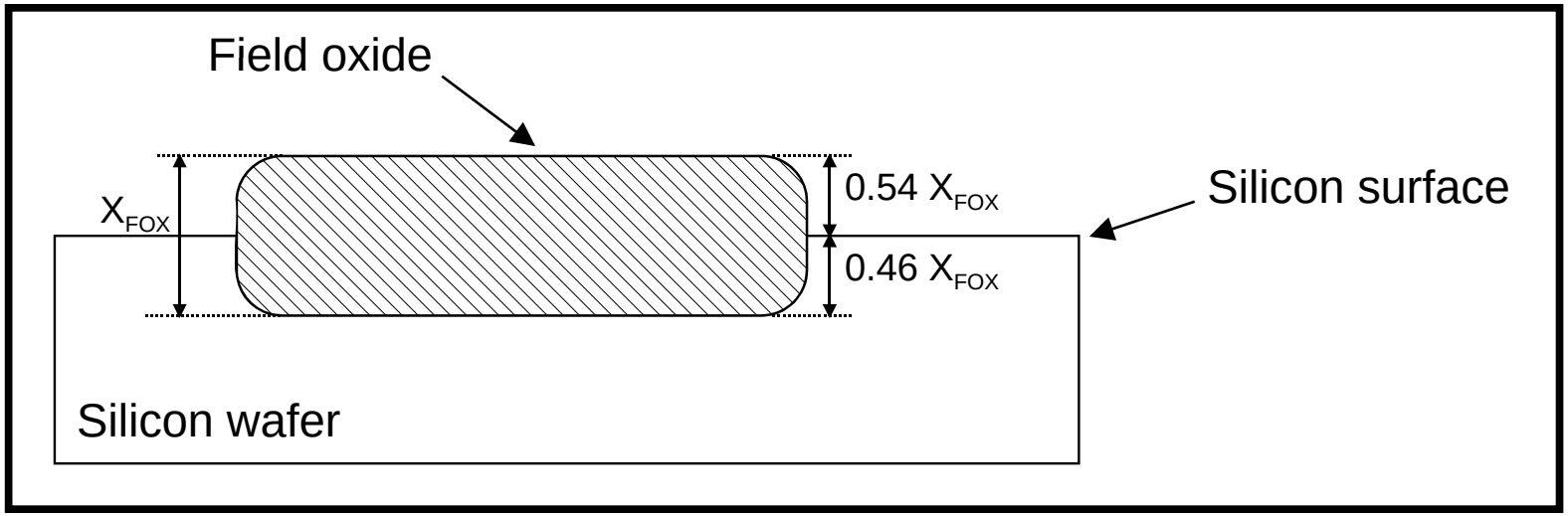
4.2 Local oxidation of silicon (LOCOS)

- The photoresist mask is removed
- The SiO_2/SiN layers will now act as a masks
- The thick field oxide is then grown by:
  - exposing the surface of the wafer to a flow of oxygen-rich gas
- The oxide grows in both the vertical and lateral directions
- This results in a active area smaller than patterned



CMOS fabrication sequence

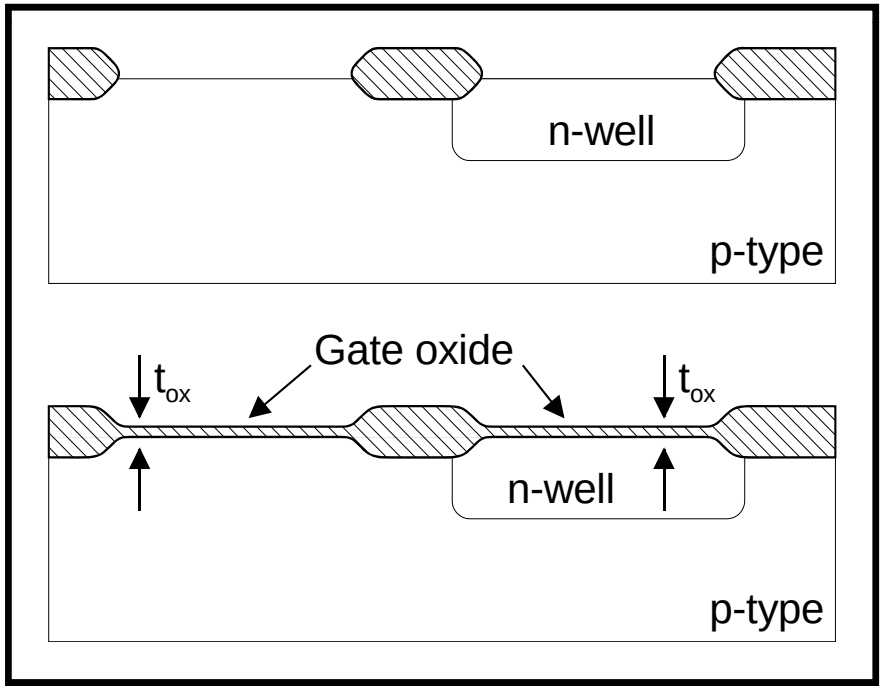
- Silicon oxidation is obtained by:
  - Heating the wafer in a oxidizing atmosphere:
    - Wet oxidation: water vapor, T = 900 to 1000ºC (rapid process)
    - Dry oxidation: Pure oxygen, T = 1200ºC (high temperature required to achieve an acceptable growth rate)
- Oxidation consumes silicon
  - SiO_2 has approximately twice the volume of silicon
  - The FOX is recedes below the silicon surface by $0.46X_{FOX}$



CMOS fabrication sequence

5. Gate oxide growth

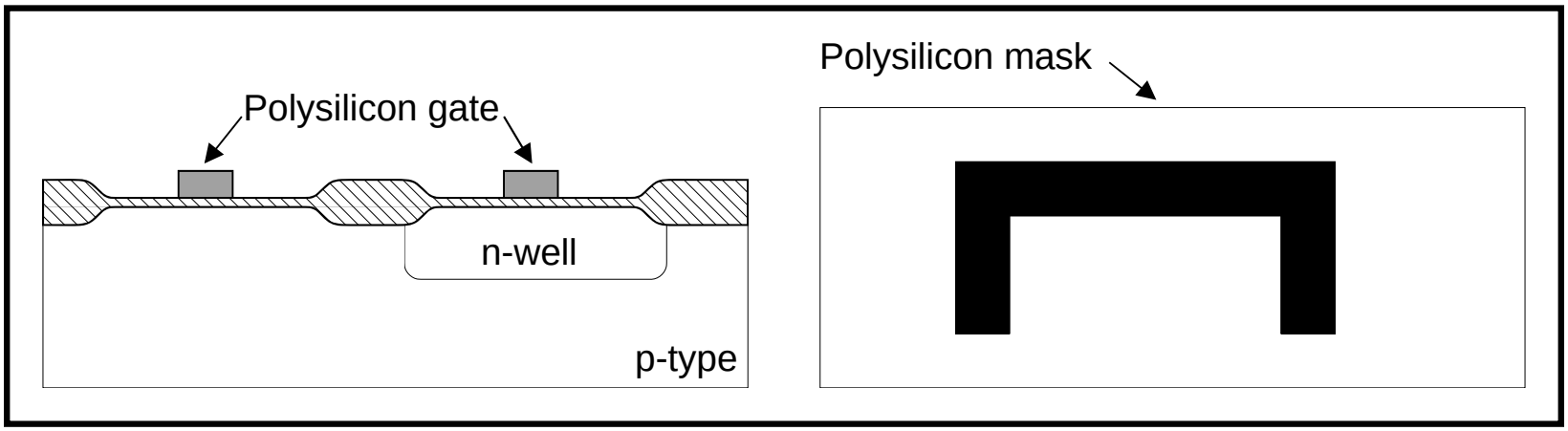
- The nitride and stress-relief oxide are removed
- The devices threshold voltage is adjusted by:
  - adding charge at the silicon/oxide interface
- The well controlled gate oxide is grown with thickness t_{ox}



CMOS fabrication sequence

6. Polysilicon deposition and patterning

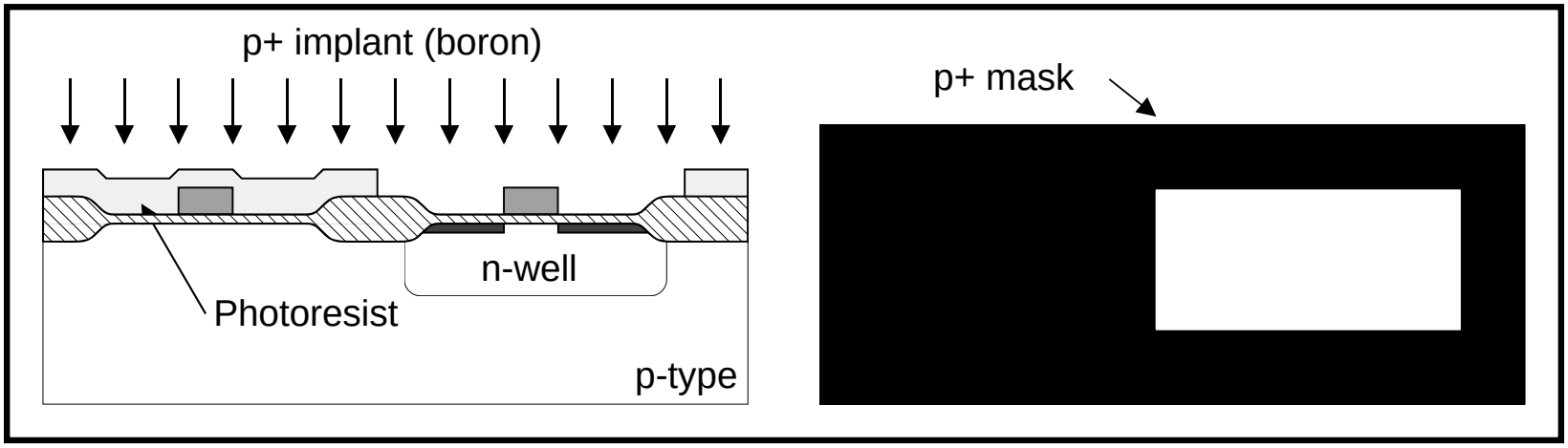
- A layer of polysilicon is deposited over the entire wafer surface
- The polysilicon is then patterned by a lithography sequence
- All the MOSFET gates are defined in a single step
- The polysilicon gate can be doped (n+) while is being deposited to lower its parasitic resistance (important in high speed fine line processes)



CMOS fabrication sequence

7. PMOS formation

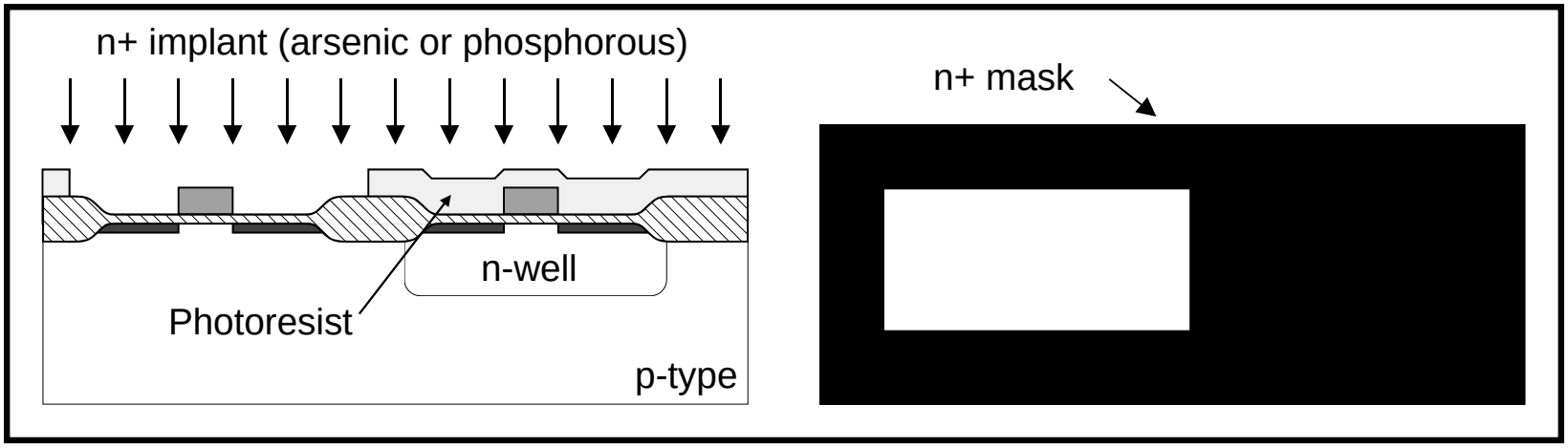
- Photoresist is patterned to cover all but the p+ regions
- A boron ion beam creates the p+ source and drain regions
- The polysilicon serves as a mask to the underlying channel
  - This is called a self-aligned process
  - It allows precise placement of the source and drain regions
- During this process the gate gets doped with p-type impurities
  - Since the gate had been doped n-type during deposition, the final type (n or p) will depend on which dopant is dominant



CMOS fabrication sequence

8. NMOS formation

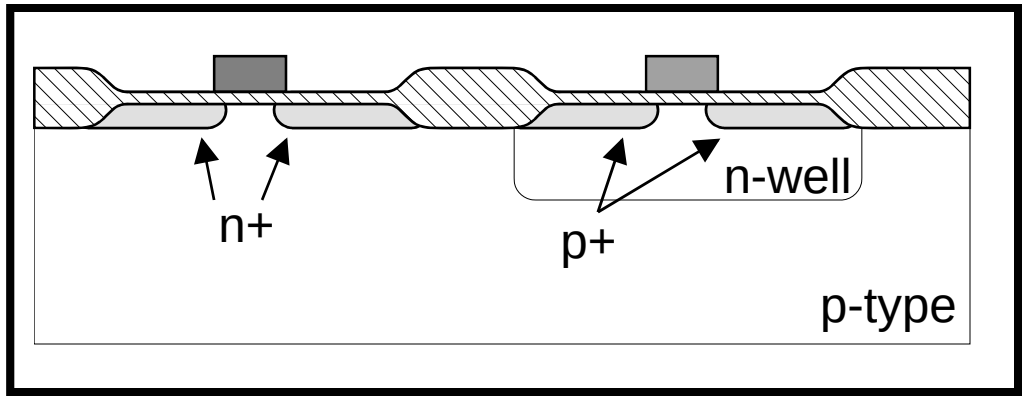
- Photoresist is patterned to define the n+ regions
- Donors (arsenic or phosphorous) are ion-implanted to dope the n+ source and drain regions
- The process is self-aligned
- The gate is n-type doped



CMOS fabrication sequence

9. Annealing

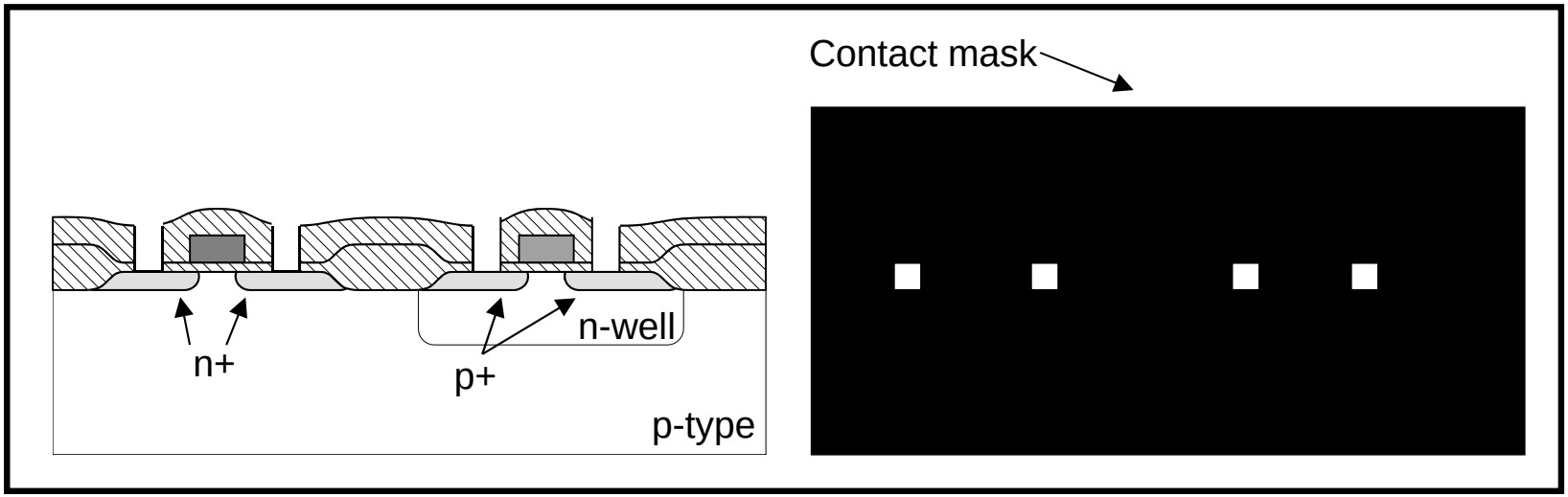
- After the implants are completed a thermal annealing cycle is executed
- This allows the impurities to diffuse further into the bulk
- After thermal annealing, it is important to keep the remaining process steps at as low temperature as possible



CMOS fabrication sequence

10. Contact cuts

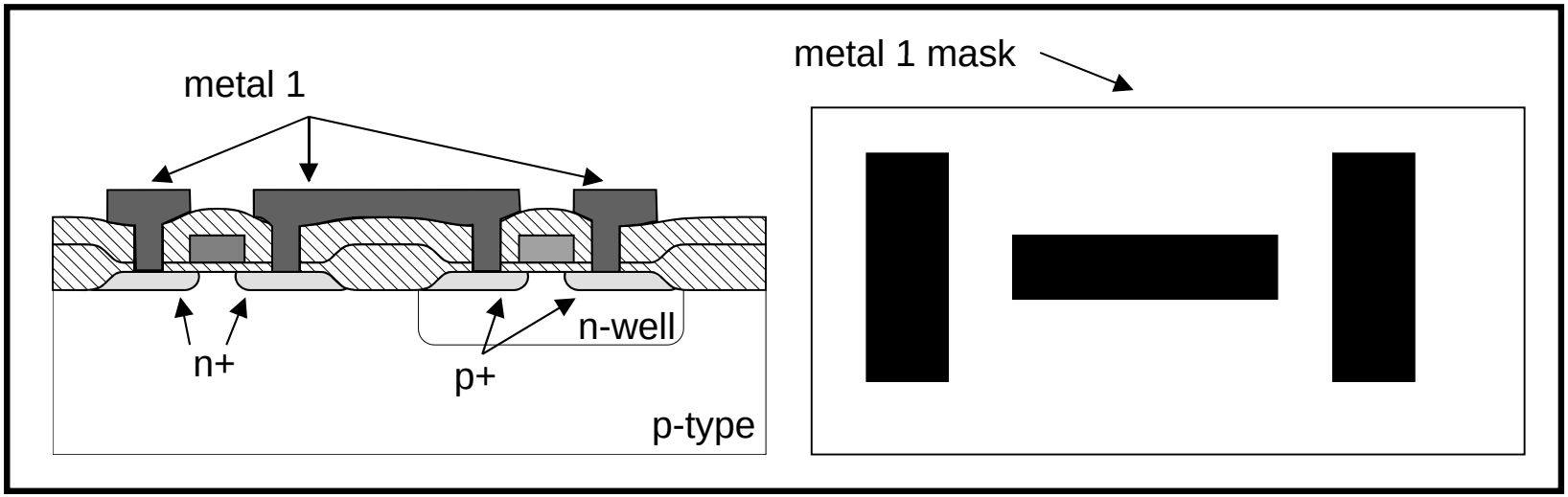
- The surface of the IC is covered by a layer of CVD oxide
  - The oxide is deposited at low temperature (LTO) to avoid that underlying doped regions will undergo diffusive spreading
- Contact cuts are defined by etching SiO_2 down to the surface to be contacted
- These allow metal to contact diffusion and/or polysilicon regions



CMOS fabrication sequence

11. Metal 1

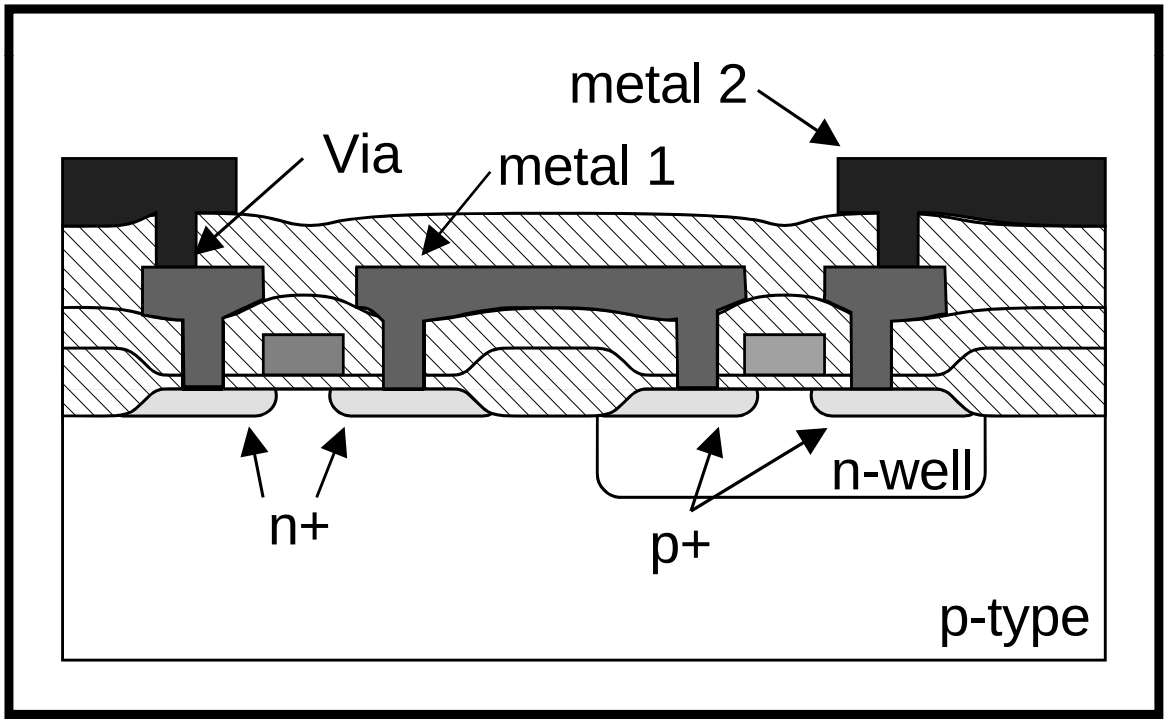
– A first level of metallization is applied to the wafer surface and selectively etched to produce the interconnects



CMOS fabrication sequence

12. Metal 2

- Another layer of LTO CVD oxide is added
- Via openings are created
- Metal 2 is deposited and patterned



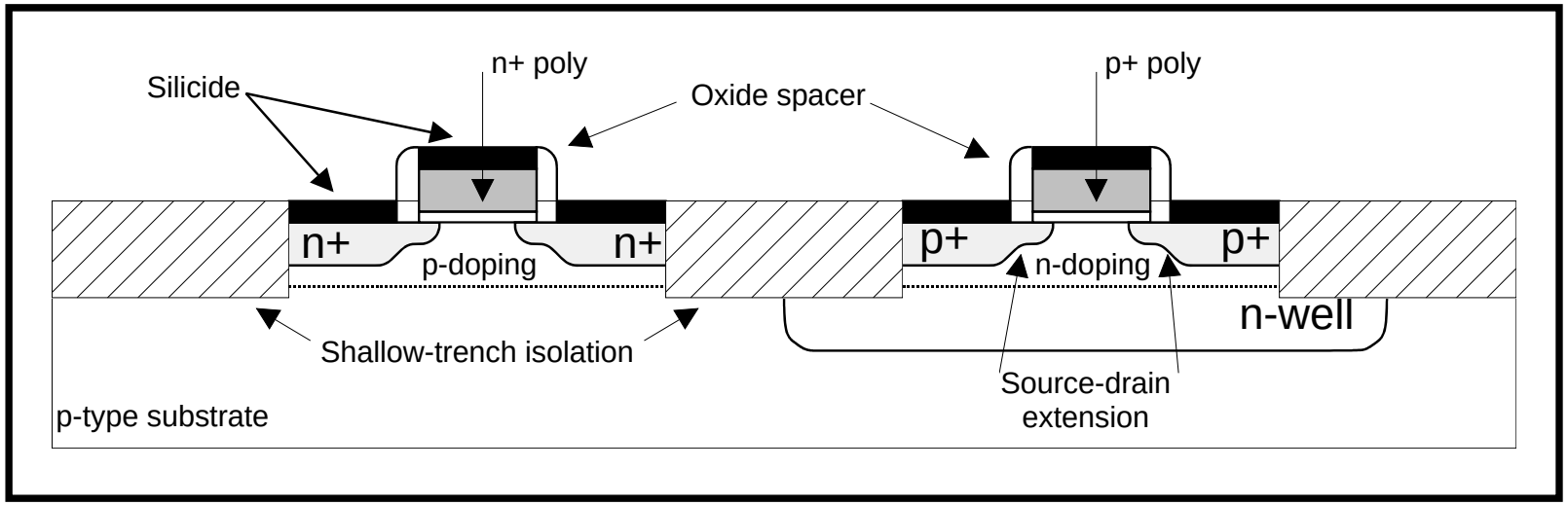
CMOS fabrication sequence

13. Over glass and pad openings

- A protective layer is added over the surface:
- The protective layer consists of:
  - A layer of SiO_2
  - Followed by a layer of silicon nitride
- The SiN layer acts as a diffusion barrier against contaminants (passivation)
- Finally, contact cuts are etched, over metal 2, on the passivation to allow for wire bonding.

Advanced CMOS processes

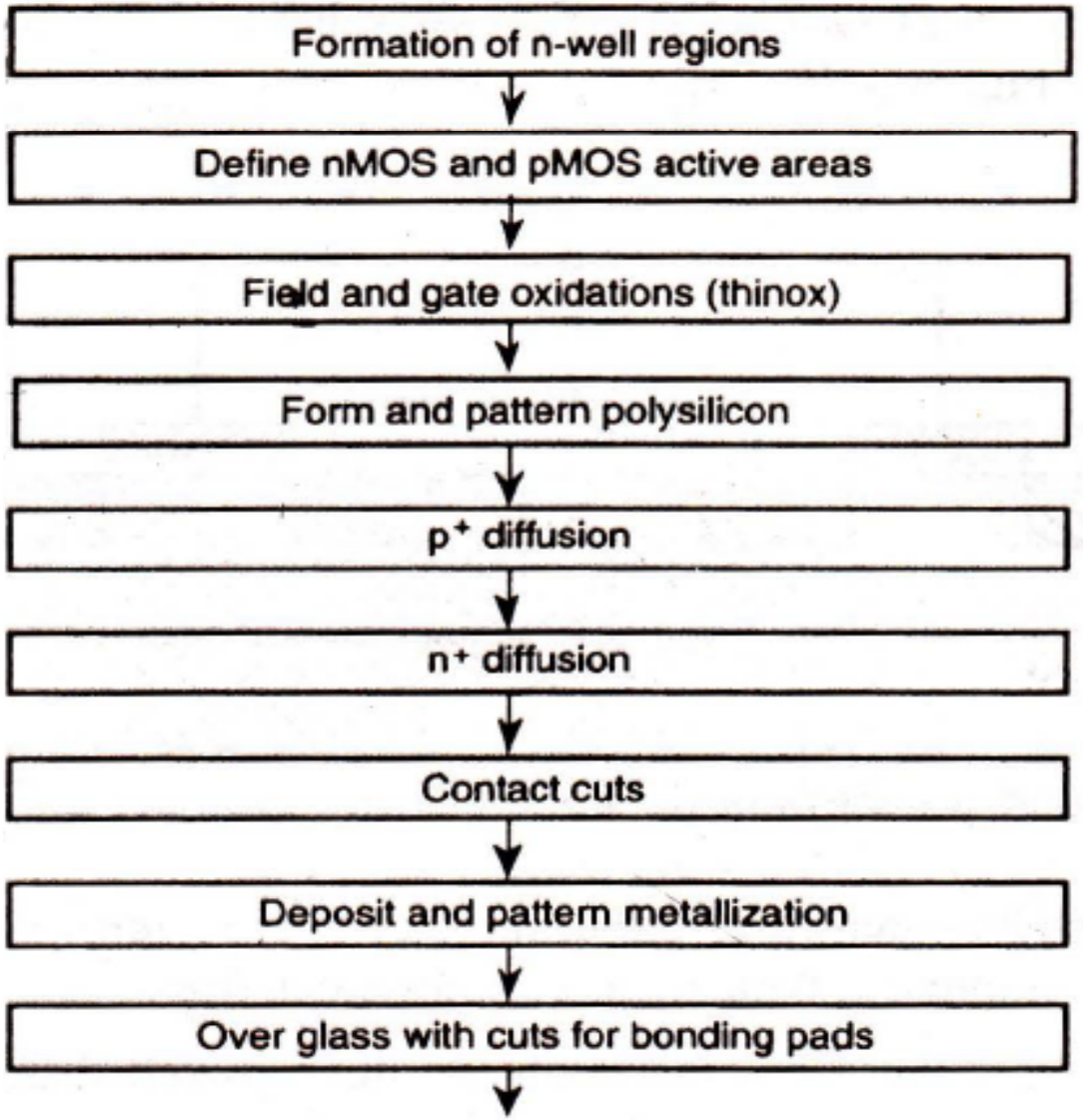
- Shallow trench isolation
- n+ and p+-doped polysilicon gates (low threshold)
- source-drain extensions LDD (hot-electron effects)
- Self-aligned silicide (spacers)
- Non-uniform channel doping (short-channel effects)



Process enhancements

- Up to eight metal levels in modern processes
- Copper for metal levels 2 and higher
- Stacked contacts and vias
- Chemical Metal Polishing for technologies with several metal levels
- For analogue applications some processes offer:
  - capacitors
  - resistors
  - bipolar transistors (BiCMOS)

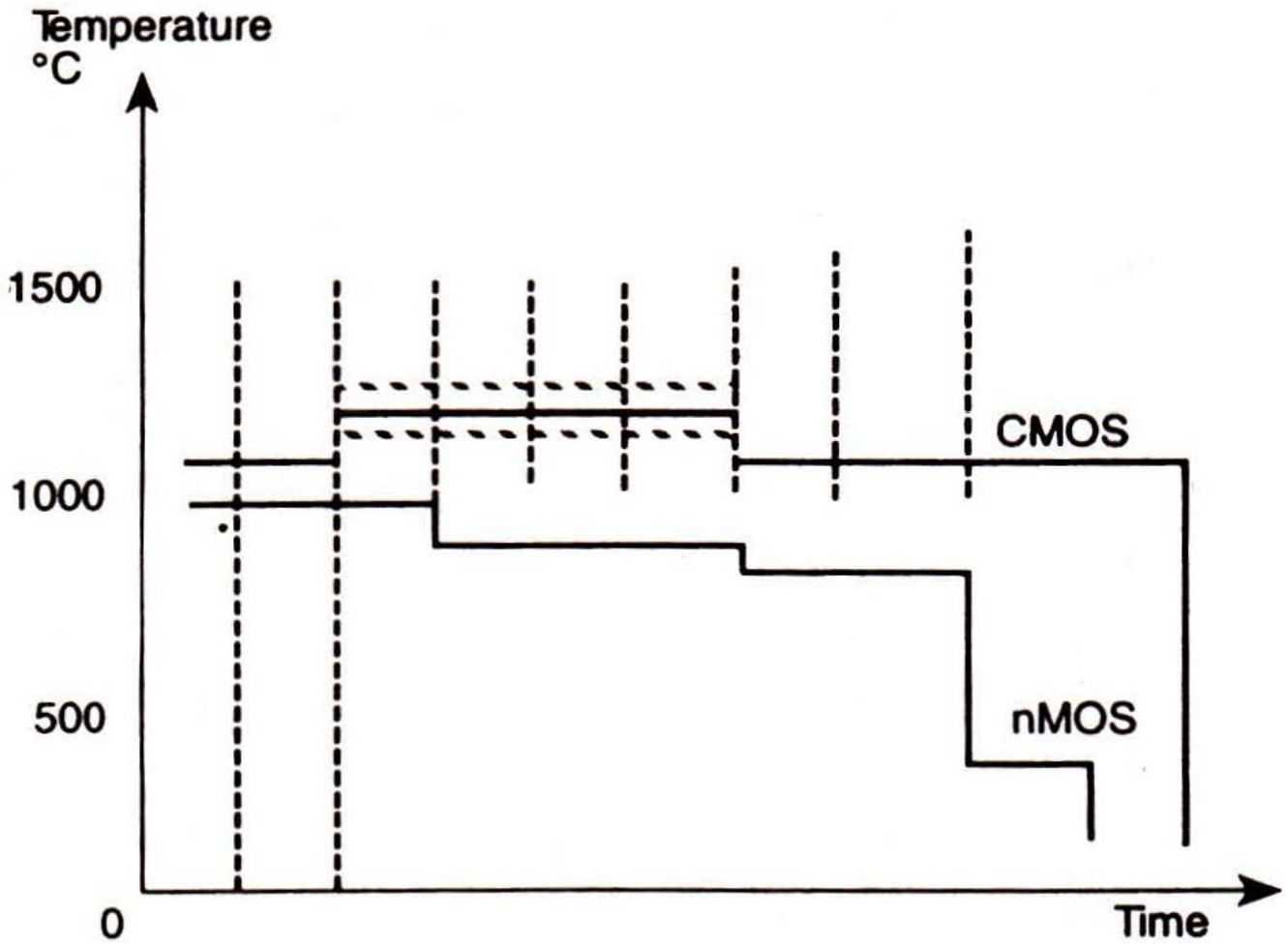
Main Step for n-well Process



THERMAL ASPECTS OF PROCESSING

- Processes involved in making nMOS and CMOS devices have differing high temperature sequences
- The CMOS p-well process, for example, has a high temperature p-well diffusion process (1100 to 1250°C),
- nMOS process having no such requirement. ·Because of the simplicity, ease of fabrication, and high density per unit area of nMOS circuits,
- many of the earlier IC designs, still in current use, have been fabricated using nMOS technology and it is likely that nMOS and CMOS system designs will continue to co-exist for some time to come.

Thermal sequence difference between nMOS and CMOS processes.



Production of masks

- masks are produced by standard optical techniques
- uses an E-beam machine.

Mask Making

- Starting material consists of chrome-plated glass plates which are coated with an E-beam sensitive resist.
- E-beam machine is loaded with the mask description data (MEBES).
- Plates are loaded into the E-beam machine, where they are exposed with the patterns specified by the customer's mask data.
- After exposure to the E-beam, the plates are introduced into a developer to bring out the patterns left by the E-beam in the resist coating.
- The cycle is followed by a bake cycle and a plasma de-summing, which removes the resist residue.
- The chrome is then etched and the plate is stripped of the remaining E-beam resist.